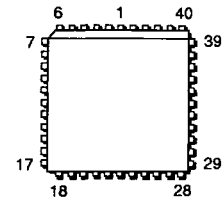
SC11481/SC11486/SC11488
32K HiColor™/80 MHz 256 Palette For Personal System/2™

SIERRA SEMICONDUCTOR

FEATURES

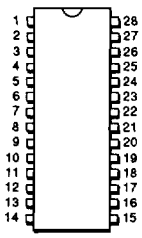
- ☐ 32K HiColor™ Mode (Hardware/Software Selectable)
- ☐ 80 MHz Pipelined Operation–Psuedo-color mode
- ☐ 40 MHz Pipelined Operation–HiColor™ Mode
- ☐ Triple 6-bit or 8-bit D/A Converters
- ☐ Supports 15-bit HiColor RGB inputs and 8-bit Pseudo-Color
- ☐ Analog Output Comparators
- ☐ On-chip Voltage Reference
- ☐ Anti-Sparkle Circuitry
- ☐ 15 Overlay Registers (SC11481/SC11488)
- ☐ 256 Word Color Palette RAM
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Sync on all Three Channels (SC11481/SC11488)
- ☐ Programmable Pedestal (SC11481/SC11488)
- ☐ Standard MPU Interface
- ☐ +5V CMOS Monolithic (EPI) Construction
- ☐ Available Clock Rates FOR Pseudo-Color
  - 80 MHz • 50 MHz
  - 66 MHz • 35 MHz

44-PIN PLCC PACKAGE



SC11481CV
SC11486CV
SC11488CV

28-PIN DIP PACKAGE



SC11486CN

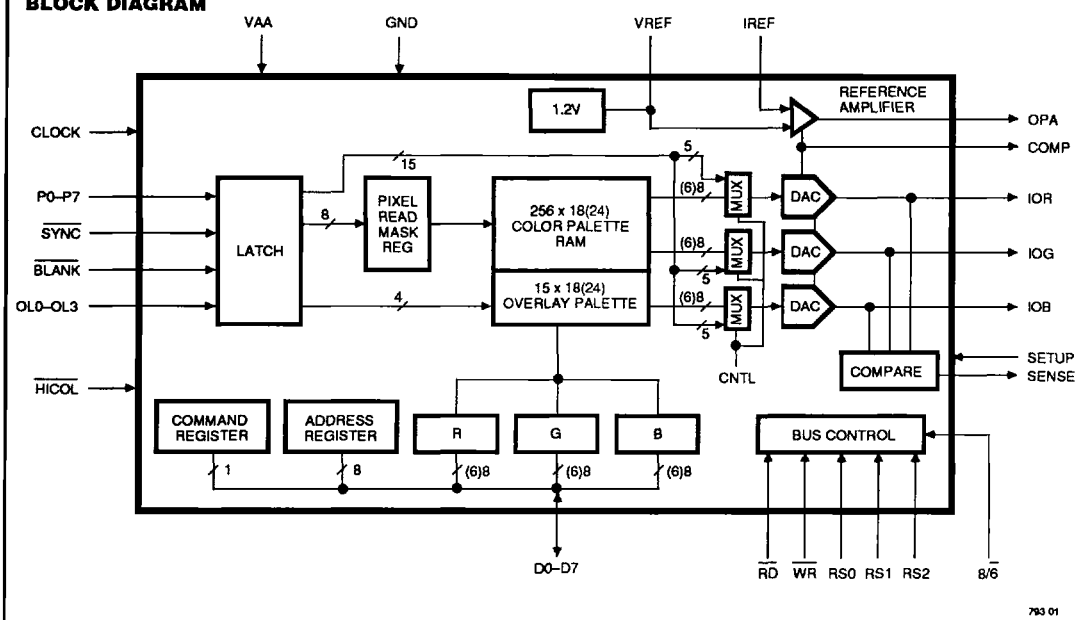
GENERAL DESCRIPTION

The SC11481, SC11486 and SC11488 are pin-compatible and software-compatible with the SC11471, SC11476 and SC11478 Color Palettes designed specifically for Personal System/2™ compatible color graphics. The SC11486 is also available in a 28-pin DIP package that is pin compatible with the IMSG171/IMSG176.

The SC11481/SC11486/SC11488 supports 15-bit HiColor™ and 8-bit pseudo-color. The HiColor™ mode provides the ability to display 32K colors simultaneously. It is specifically tailored to work with the Tseng Labs ET4000 VGA controller chip in the high-color mode.

The SC11481 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The SC11488 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It

BLOCK DIAGRAM



793 01

Personal System/2 is a trademark of IBM.

may be configured for either 6 bits or 8 bits per color operation.

The SC11481 and SC11488 also include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels, a programmable pedestal (0 or 7.5IRE), and use of either an external voltage or current reference is also supported.

The SC11486 is similar to the SC11481, but has no overlays or sync information on the analog outputs.

On-chip analog comparators are included to simplify diagnostics and debugging, with the resulting output onto the SENSE pin. Also included is an on-chip voltage reference to simplify using the device.

When the HiColor™ mode is not activated, SC11481/486/488 behave exactly as SC11471/476/478 with anti-sparkle capabilities, on chip voltage/current reference, and analog comparators.

The SC11481/486/488 generate RS-343A compatible red, green, and blue video signals, and are capable of driving doubly-terminated 75 Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75 Ohm load, without requiring external buffering.

FUNCTIONAL DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the SC11481/486/488 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, command registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address register (RAM write mode)
0	1	1	Address register (RAM read mode)
0	0	1	Color palette RAM
0	1	0	Pixel read mask register
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay registers
1	1	0	Command Register

Table 1. Control Input Truth Table

Writing Color Palette RAM and Overlay Color Data

To write color data, the MPU writes the address register (selecting RAM write or overlay write mode) with the address of either the color palette RAM location or the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the SC11481/486) and written to the location specified by the address register. The address register then increments to the next location which MPU may modify by simply writing another sequence of red, green and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM and Overlay Color Data

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the contents of the color palette RAM or the contents of the overlay location specified by the address register are copied into the R, G, B registers and the address register gets incremented again. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses.

To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMS or the overlay registers, an internal anti-sparkle logic is implemented to maintain the previous output color data on the three D/A Converters output while the transfer between the color look-up table RAMS and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

SC11481/486 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

SC11488 Data Bus Interface

On the SC11488, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8-bits (8/$\overline{6}$ = logical one) or 6-bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the SC11481/486), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the SC11488's full scale output current will be about 1.5% lower than when it is in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being logic zero in the 6-bit mode.

Color Modes

Two color modes are supported by the SC11481/486/488: 8-bit psuedo-color and 16-bit high-color. The mode of operation is determined either by the command register or by the $\overline{\text{HICOL}}$ pin.

HiColor™ Mode

When the HiColor™ mode is activated, the input stage accepts 16-bits of pixel information from the pixel select lines P0-P7, by latching the lower 8 bits on the rising edge, and the upper 8 bits on the falling edge of the pixel clock. The two bytes form a 16 bit word which is used as a direct input to the triple video DACs. The color palette RAM and pixel read mask register are bypassed.

HiColor™ Mode Data Format

The data captured on the rising edge of the pixel clock constitute the LSB (B7-B0) and the data captured on the falling edge of the pixel clock constitute the MSB (B15-B8) bytes of the color data. The 16 bit word (B15-B0) is assigned to the color DACs in the following format:

B14 - B10	Red DAC
B7 - B5	Green DAC
B4 - B0	Blue DAC
B15	Ignored

The three LSBs of all three DACs are forced to zero.

SENSE Output

SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ±10% when using the internal voltage reference or an external current reference. Note that SYNC should be logical zero for SENSE to be stable.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the SC11481/486) of color information to the three D/A converters.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 4 and 5 detail how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. Note that the SC11476 generates only a 0 IRE blanking pedestal (Figure 2).

The analog outputs of the SC11481/486/488 are capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

Command Register

This register is active in all modes. It may be written to or read by the MPU at any time and is initialized to a logical zero after the power on reset.

D7	HiColor™ mode	A logical one will activate the HiColor™ mode. A logical zero will set it in the psuedo-color mode.
D6-D0	Not used	

In the SC11486, where the RS2 pin is not available, the command register is accessed by using the following special sequence of events:

A flag will be set when the pixel read mask register (RS1 = 1 & RS0 = 0) is read four times consecutively. The next write to the pixel mask register will be directed to the command register and can be used to set the D7 bit of the command register. A write to any address or a read from any address other than the pixel read mask register will reset the flag. This flag will also get reset after the power on reset.

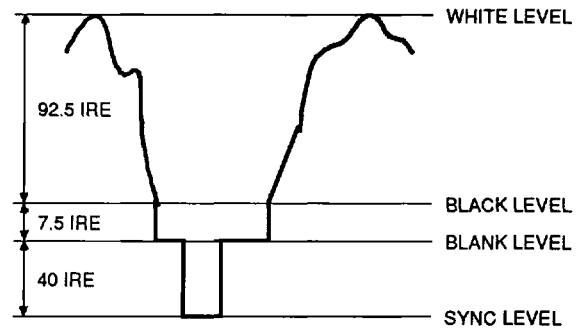
	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				Red value Green value Blue value
ADDR0–7 (counts binary)	$00-$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	Color palette RAM Reserved Overlay Color 1 : Overlay Color 15

Table 2. Address Register (ADDR) Operation

OL0–OL3	P0–P7	Addressed by Frame Buffer
$0	$00	Color Palette RAM Location $00
$0	$01	Color Palette RAM Location $01
:	:	:
$0	$FF	Color Palette RAM Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

SC11481/488 w/o SYNC		SC11481/488 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

793 03

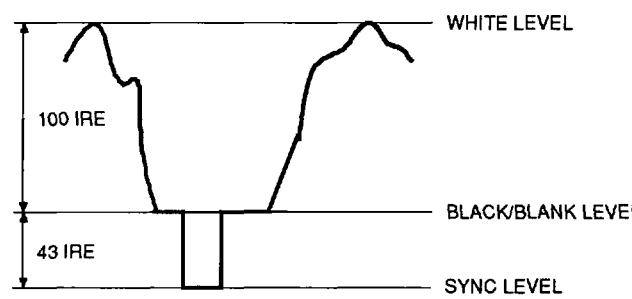
Figure 1. Composite Video Output Waveforms (SETUP = VAA)

Description	SC11481/488 IOUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω.

Table 4. Video Output Truth Table (SETUP = VAA)

SC11486 or SC11481/488 w/o Sync		SC11481/488 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.256
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = GND. VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

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Figure 2. Composite Video Output Waveforms (SETUP = GND)

Description	SC11486 IOUT (mA)	SC11481/488 IOUT (mA)	SYNC	BLANK	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA–SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω.

Table 5. Video Output Truth Table (SETUP = GND)

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
BLANK	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal.
SYNC	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). SYNC does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC, and BLANK inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable.
SENSE	Sense output (TTL compatible). SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE may not be stable while SYNC is toggling.
HICOL	HiColor Mode select input (TTL compatible). A logic zero will enable the HiColor mode. The HICOL pin should be tied to VAA to disable hardware selection of the HiColor mode.

<table>
<tr><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>IREF</td><td>Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current.

When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is:

RSET (Ω) = K • 1000 • VREF (V)/Iout (mA)

K is defined in the table below for doubly-terminated 75 Ω loads.

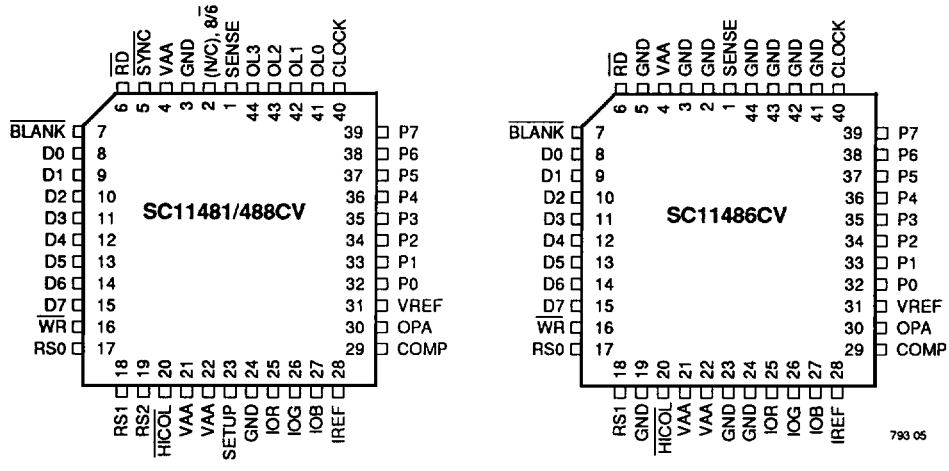
When using an external current reference (Figures 4 and 5) the relationship between IREF and the full scale output current on each output is:

IREF (mA) = Iout (mA)/K

<table>
<tr><th>Part Number</th><th>Mode</th><th>Pedestal</th><th>K</th></tr>
<tr><td>SC11488</td><td>6-bit
8-bit
6-bit
8-bit</td><td>7.5 IRE
7.5 IRE
0.0 IRE
0.0 IRE</td><td>3.170
3.195
3.000
3.025</td></tr>
<tr><td>SC11481</td><td>6-bit</td><td>7.5 IRE
0.0 IRE</td><td>3.170
3.000</td></tr>
<tr><td>SC11486</td><td>6-bit</td><td>0.0 IRE</td><td>2.100</td></tr>
</table>
</td></tr>
<tr><td>COMP</td><td>Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.</td></tr>
<tr><td>VREF</td><td>Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.

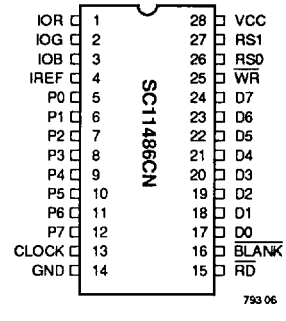
When using internal reference this pin should not drive any external circuitry except for the decoupling capacitor.</td></tr>
<tr><td>OPA</td><td>Reference amplifier output. If an external voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.</td></tr>
<tr><td>VAA</td><td>Analog power. All VAA pins must be connected.</td></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected.</td></tr>
<tr><td>$\overline{WR}$</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.</td></tr>
<tr><td>$\overline{RD}$</td><td>Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation RS2 being performed, as illustrated in Tables 1 and 2.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>8/$\overline{6}$</td><td>8-bit/$\overline{6}$-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant bit during color read/write cycles (D6 and D7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC11488.</td></tr>
</table>

CONNECTION DIAGRAM



44-Pin PLCC

N/C pins may be left unconnected without affecting the performance of the SC11481/486/488. Names in parentheses are pin names for SC11481.



28-Pin DIP

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the SC11481/486/488 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all SC11481/486/488 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the SC11481/486/488, the analog output traces, and all the digital signal traces leading up to the SC11471/476/478.

Power Planes

The SC11481/486/488 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 3, 4 and 5. This bead should be located within three inches of the SC11481/486/488.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SC11481/486/488 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that

portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the SC11481/486/488 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the SC11481/486/488 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the SC11481/486/488 should be avoided to reduce noise pickup.

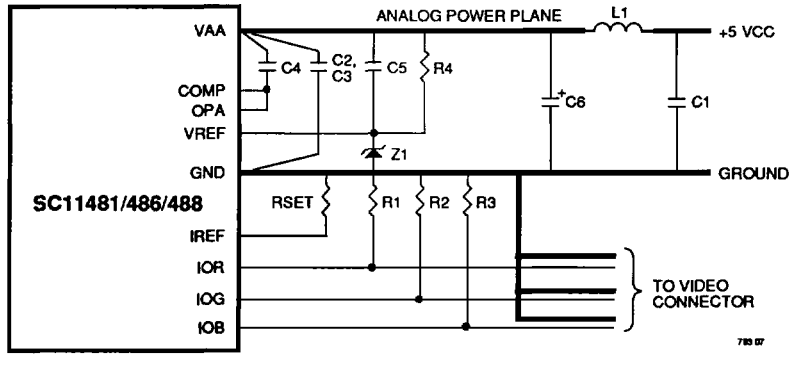
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane, and not the analog power plane.

Analog Signal Interconnect

The SC11481/486/488 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

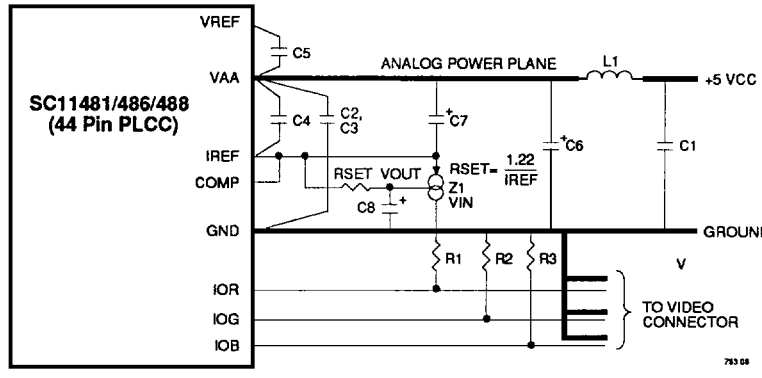
For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the SC11481/486/488 to minimize reflections.



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385BZ-1.2
R4	1K Ω 5% Resistor	

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11481/486/488.

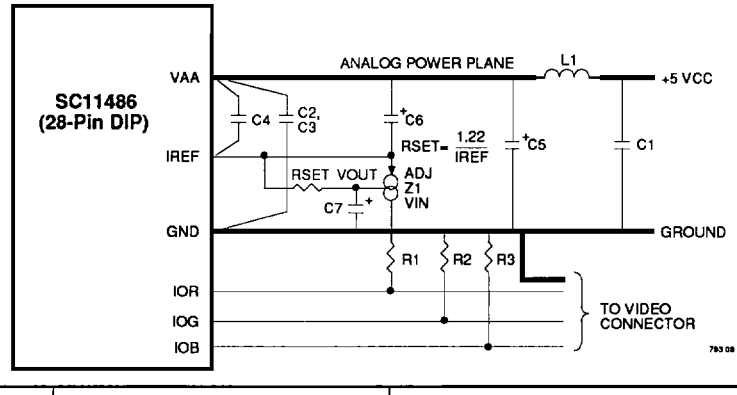
Figure 3. Typical Connection Diagram and Parts List (External Voltage Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C7	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C8	1 µF Capacitor	Mallory CSR13G105KM
RSET	1% Metal Film Resistor	Dale CMF-55C
L1	Ferrite Bead	Fair-Rite 2743001111
Z1	Adjustable Regulator	National Semiconductor LM337LZ
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11481/486/488.

Figure 4. Typical Connection Diagram and Parts List (External Current Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C5	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C6	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C7	1 µF Capacitor	Mallory CSR13G105KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	Adjustable Regulator	National Semiconductor LM337LZ
RSET	1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11876.

Figure 5. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS

VAA (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to VAA + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply (VAA)				
80, 66 MHz PRVTS	+4.75	5.0	5.25	V
50, 35 MHz PRVTS	+4.5	5.0	5.5	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (VREF)	+1.14	1.235	1.26	V
Current Reference (IREF)				
Standard RS-343A	–3	–8.39	–10	mA
PS/2 Compatible	–3	–8.88	–10	mA

3

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC11488		8	8	8	Bits
SC11481/486		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC11488				±1	LSB
SC11486				±1/2	LSB
SC11481				±1/4	LSB
Differential Linearity Error	D_L				
SC11488				±1	LSB
SC11486				±1/2	LSB
SC11481				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND–0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC11481/488					
SETUP = VAA		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC11486		0	0	0	µA
Blank Level					
SC11481/488		6.29	7.62	8.96	mA
SC11486		0	5	50	µA
Sync Level (SC11481/488 only)		0	5	50	µA
LSB Size					
SC11488 (8/$\overline{6}$ = Logical One)			69.1		µA
SC11481/486			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedence	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / %ΔVAA

ANALOG OUTPUT LEVELS—P/S 2 COMPATIBILITY

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC11481/488					
SETUP = VAA		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
SC11486		0	5	50	µA
Blank Level					
SC11481/488		6.6	8	9.4	mA
SC11486		0	5	50	µA
Sync Level (SC11481/488 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11486, IREF = –8.88 mA.

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11486, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the SC11481/486 have 6-bit DACs (and the SC11478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	80 MHZ DEVICES MIN	80 MHZ DEVICES TYP	80 MHZ DEVICES MAX	66 MHZ DEVICES MIN	66 MHZ DEVICES TYP	66 MHZ DEVICES MAX	UNITS
Clock Rate (Pseudo Color)	Fmax			80			66	MHz
Clock Rate (HiColor™ Mode)	Fmax(HC)			40			40	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Pixel and Control Setup Time LSB (HiColor™ Mode)	20	-1.0			-1.0			ns
Pixel and Control Hold Time LSB (HiColor™ Mode)	21	7.0			7.0			ns
Pixel and Control Setup Time MSB (HiColor™ Mode)	22	-1.0			-1.0			ns
Pixel and Control Hold Time MSB (HiColor™ Mode)	23	7.0			7.0			ns
Clock Cycle Time (P13)	13	12.5			15.5			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Clock Cycle Time (HiColor™ Mode)	13	25			25			ns
Clock Pulse Width High Time (HiColor™ Mode)	14	9			9			ns
Clock Pulse Width Low Time (HiColor™ Mode)	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			15		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV-sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE Output Delay	19		1			1		µs
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on page 706.

		50 MHZ DEVICES			35 MHZ DEVICES			
PARAMETER	**SYMBOL**	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Clock Rate (Pseudo Color)	Fmax			50			35	MHz
Clock Rate (HiColor™ Mode)	Fmax(HC)			35			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Pixel and Control Setup Time LSB (HiColor™ Mode)	20	-1.0			-1.0			ns
Pixel and Control Hold Time LSB (HiColor™ Mode)	21	7.0			7.0			ns
Pixel and Control Setup Time MSB (HiColor™ Mode)	22	-1.0			-1.0			ns
Pixel and Control Hold Time MSB (HiColor™ Mode)	23	7.0			7.0			ns
Clock Cycle Time (P13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Clock Cycle Time (HiColor™ Mode)	13	28			28			ns
Clock Pulse Width High Time (HiColor™ Mode)	14	9			9			ns
Clock Pulse Width Low Time (HiColor™ Mode)	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV–sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE Output Delay	19		1			1		µs
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on the next page.

Test conditions: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of SC11486, IREF = -8.39 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figures 6 and 7.

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

** At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

TIMING WAVEFORMS

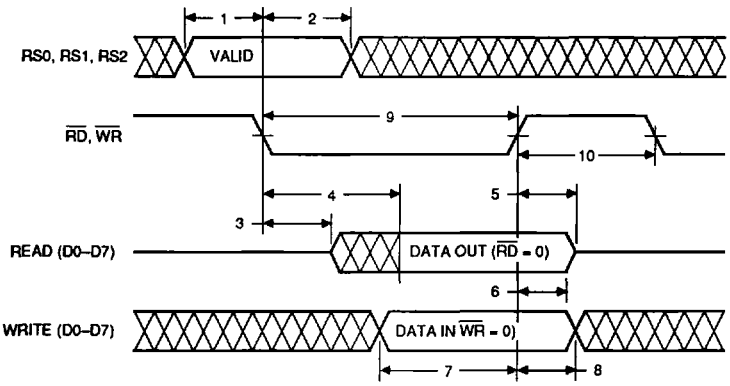
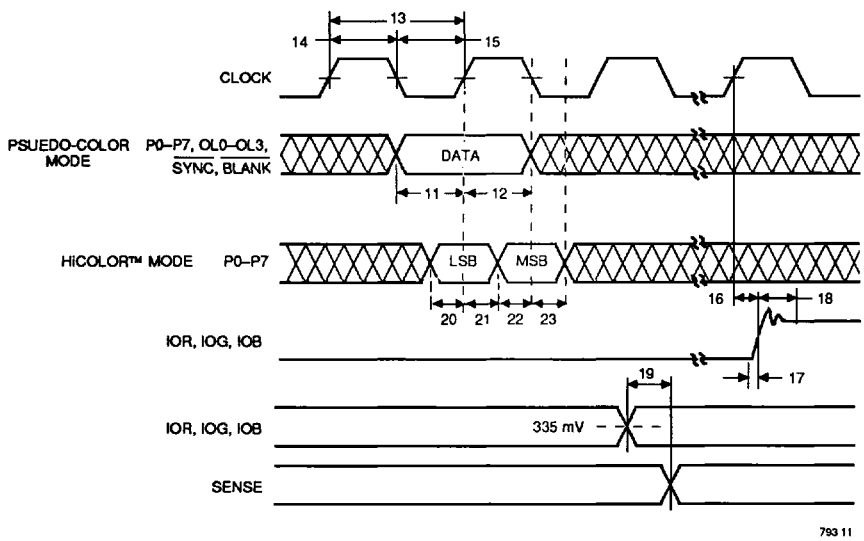


Figure 6. MPU Read/Write Timing



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB. (SC11488), ± 1/4 LSB (SC11481), or ± 1/2 LSB (SC11486).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing

ORDERING INFORMATION

PART NO.	COLOR PALETTE RAM	OVERLAY PALETTE	SYNC. GENERATION	SPEED PSEUDO	SPEED HiCOLOR	PACKAGE	AMBIENT TEMP. RANGE
SC11481CV-80	256 x 18	15 x 18	yes	80 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-66	256 x 18	15 x 18	yes	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-50	256 x 18	15 x 18	yes	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-35	256 x 18	15 x 18	yes	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-66	256 x 18	–	no	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-50	256 x 18	–	no	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-35	256 x 18	–	no	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CN-66	256 x 18	–	no	66 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11486CN-50	256 x 18	–	no	50 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11486CN-35	256 x 18	–	no	35 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11488CV-80	256 x 24	15 x 24	yes	80 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-66	256 x 24	15 x 24	yes	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-50	256 x 24	15 x 24	yes	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-35	256 x 24	15 x 24	yes	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.