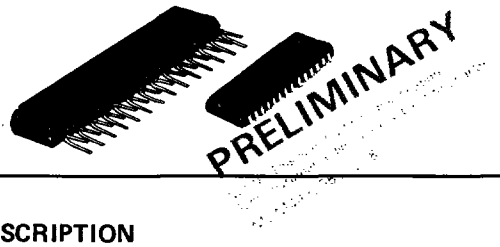
M5M442256J, L-8, -10, -12

1048576-BIT DUAL-PORT DYNAMIC RAM



DESCRIPTION

The Mitsubishi M5M442256J, L is a high speed 1048576-bit Dual Port Dynamic Memory equipped with a 256K x 4 Dynamic RAM Port and a 512 x 4 Serial Read/Write Port. The use of triple-layer polysilicon CMOS process combined with silicide technology and a single transistor dynamic storage cell provide both high circuit density and low power dissipation.

The Serial Read/Write Ports are connected to an internal 2048 bit Data Register through a 512 x 4 Serial Input/Output Control circuit and can be serially readout or written in with a clock rate of up to 33MHz.

All reads and writes are done relative to the RAM array, thus Data transfer from the RAM array to the Data Register is referred to as a Read Transfer, while Data Transfer from the Data Register to the RAM array is referred to as a Write Transfer.

FEATURES

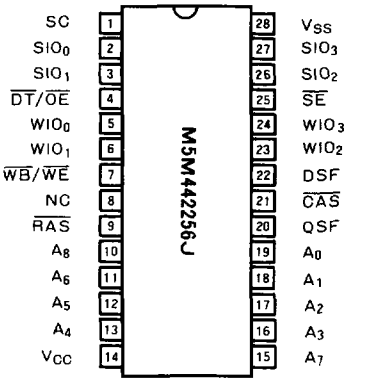
Type name	$\overline{RAS}$ Access Time (ns)	Random Read/Write Cycle Time (ns)	Serial Read Cycle Time (ns)	Random Read V_{CC} Supply Current (mA)	Serial Read/Write V_{CC} Supply Current (mA)
M5M442256J, L-8	80	160	30	80	60
M5M442256J, L-10	100	190	30	70	50
M5M442256J, L-12	120	220	40	60	40

- Dual Port Architecture
  - RAM Port: 256K-word x 4-bit
  - Serial Port: 512 word x 4-bit
- Bidirectional Data Transfer function between the RAM array and the Data Register.
- Fully Asynchronous Dual Port Accessability (Split SAM)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function
- Real Time Data Transfer from the RAM Array to the Data Register.
- Fast Page Mode, Hidden Refresh and $\overline{CAS}$ before $\overline{RAS}$ Refresh.
- 512 cycle/8ms Refresh.
- Flash write operation.
- Block write operation

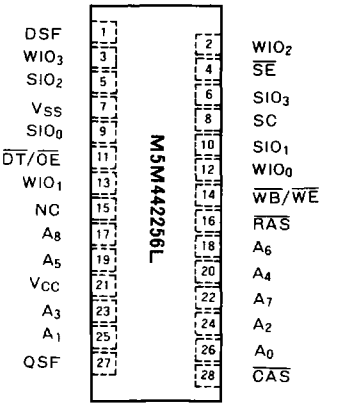
APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VTR, Videotex, Teletext, Video printer, High Speed data transmission systems.

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K (400 mil 28 pin SOJ)



Outline 28P5L (400 mil 28 pin ZIP)

NC: NO CONNECTION

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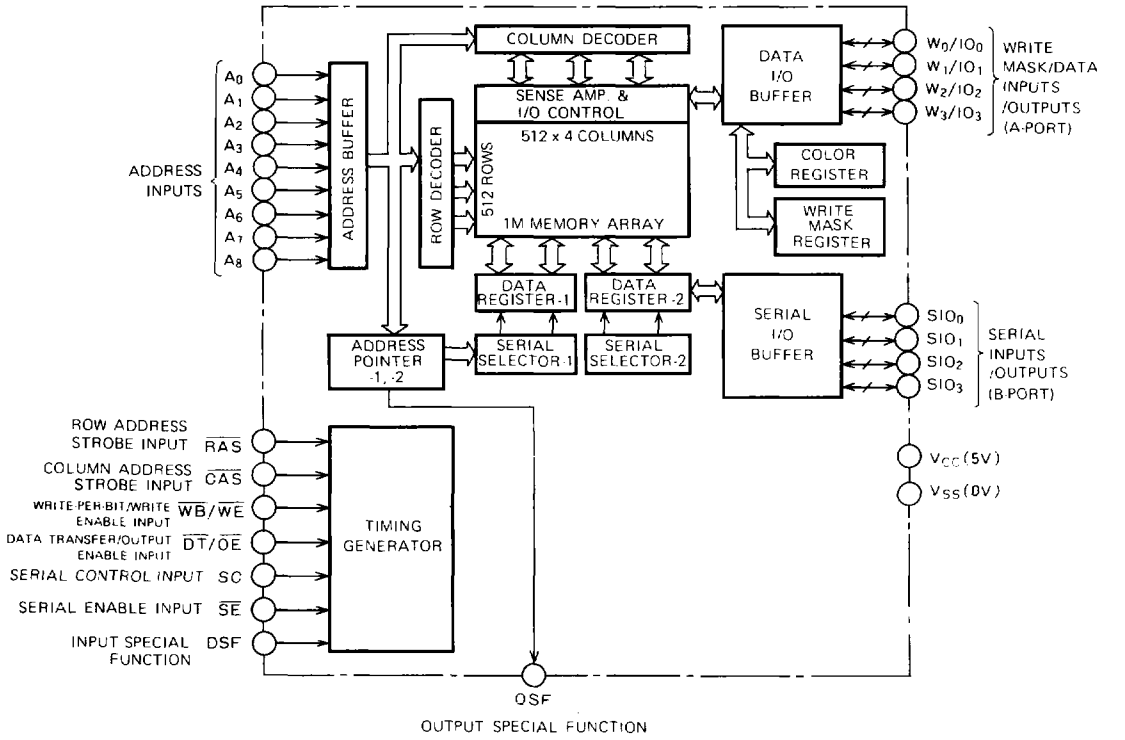
BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address (A_0~A_8) and selects the word line. It also latches the mask data for write-per-bit, flash write, write transfer and split write transfer function when the $\overline{WB}$ level is low. $\overline{CAS}$ before $\overline{RAS}$ refresh mode is available by preceeding $\overline{CAS}$ low.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address (A_9~A_{17}) and initiates the reading or writing of the selected words. In the data transfer cycle this latches the SAM Top Address Point. (TAP)
A_0~A_8	ADDRESS INPUT	The M5M442256 utilizes an address multiplex method for selecting one word among the 256K-word memory cells. 9 row addresses and 9 column addresses are latched by the $\overline{RAS}$ and $\overline{CAS}$ falling edge. In the data transfer cycle, this RAM address input is also combined with the serial access start address. (TAP)
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT / WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level is low at the $\overline{RAS}$ falling edge, Write-per-bit (RAM write with Mask) or Write transfer with MASK or Flash write with MASK cycle is selected. When it is high, normal read/write or Read transfer or Load color register cycle is selected. This clock also controls early/late write mode at the $\overline{CAS}$ falling edge.
$\overline{DT}/\overline{OE}$	DATA TRANSFER/ OUTPUT ENABLE INPUT	In RAM read cycle, it makes the data output (RAM port) enable. Also when the $\overline{DT}/\overline{OE}$ level is low at the $\overline{RAS}$ falling edge, the data transfer cycle is selected and when it is high, RAM read/write cycle or Load color register cycle or Flash write cycle is activated according to the $\overline{WB}/\overline{WE}$ and the DSF conbination.
WIOn*	WRITE MASK / DATA INPUT / OUTPUT	These are the data input/output pins to the RAM. During RAM write-per-bit cycle/split write transfer cycle/ flash write cycle, the high data pin at the $\overline{RAS}$ falling edge enables the selected-bit (row) write operation. In Write cycle, the data is latched at the late falling edge of the $\overline{CAS}$ or the $\overline{WB}/\overline{WE}$ input, whichever is the later.
SC	SERIAL CONTROL INPUT	The serial access is initiated from the SC clock rising edge. In the serial read cycle, the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
SIOn*	SERIAL INPUT / OUTPUT	512 x 4 word serial data input/output pins
$\overline{SE}$	SERIAL ENABLE INPUT	This enables the serial input/output. In the write transfer cycle, when $\overline{SE}$ is high at the $\overline{RAS}$ falling edge, Peudo transfer cycle is selected, and when it is low, Write transfer cycle is selected.
DSF	INPUT SPECIAL FUNCTION	This input defines special functions such as Split read/write transfer, Flash write, Block write and Load color register. When it is low grounded, the device works as a basic dual-port memory except for the Normal write transfer cycle masking mode.
QSF	OUTPUT SPECIAL FUNCTION	Output indicating the serial data selector status.

Note *: n = 0 ~ 3

256Kx4 Truth Table

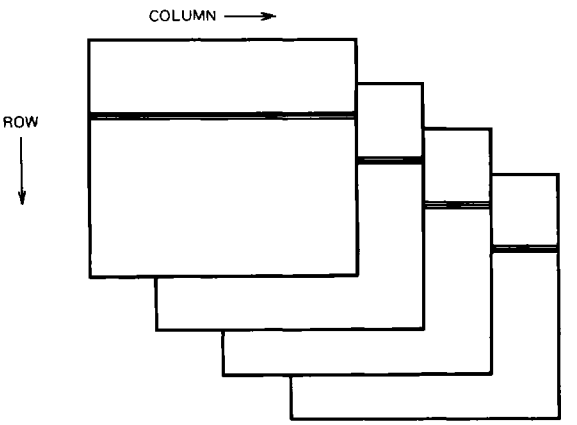
Code mnemonic	RAS falling edge							CAS falling edge				Write mask op.	Raster op.	Register			
	CAS	DT/OE	WB/WE	DSF	SE	Addr	WIOn	WB/WE	DSF	Addr	WIOn			Write mask temporary	Write mask persistant	Color	
Option	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	None use
	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
CBR	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
	0	0	1	1	—	—	—	—	—	—	—						
CBR	0	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
	0	1	0	1	—	—	—	—	—	—	—						
CBR	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	C.B.R
	0	1	1	1	—	—	—	—	—	—	—						
MWT/PWT	1	0	0	0	0/1	Row/Ref	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Wr. transfer (SE=0) Pseudo write transfer (SE=1)
	1	0	0	0	0/1	Row/Ref	WM1	—	1	TAP	—						
SWT	1	0	0	1	—	Row	WM1	—	0	TAP	—	Yes per row	—	Load use	—	—	Split write transfer with new mask
	1	0	0	1	—	Row	WM1	—	1	TAP	—						
RT	1	0	1	0	—	Row	—	—	0	TAP	—	—	—	—	—	—	Read transfer
	1	0	1	0	—	Row	—	—	1	TAP	—						
SRT	1	0	1	1	—	Row	—	—	0	TAP	—	—	—	—	—	—	Split read transfer
	1	0	1	1	—	Row	—	—	1	TAP	—						
RWNM	1	1	0	0	—	Row	WM1	*E/L	0	Col.	DQin	Yes	—	Load use	—	—	RAM write with new mask
BWNM	1	1	0	0	—	Row	WM1	—	1	Col.	Sel.	Yes	—	Load use	—	Use	Block write with new mask
FWT	1	1	0	1	—	Row	WM1	—	0	—	—	Yes per row	—	Load use	—	—	Flash write with new mask
	1	1	0	1	—	Row	WM1	—	1	—	—						
RW	1	1	1	0	—	Row	—	*E/L	0	Col.	DQin	—	—	—	—	—	R/W
BW	1	1	1	0	—	Row	—	—	1	Col.	Sel.	—	—	—	—	Use	Block write with no mask
LCR	1	1	1	1	—	Ref	—	*E/L	0	—	CLR.	—	—	—	—	Load	Load color reg.
	1	1	1	1	—	Ref	—	*E/L	1	—	CLR.						

* E/L: Early write/Late write ** Ref: Refresh Address

FUNCTION

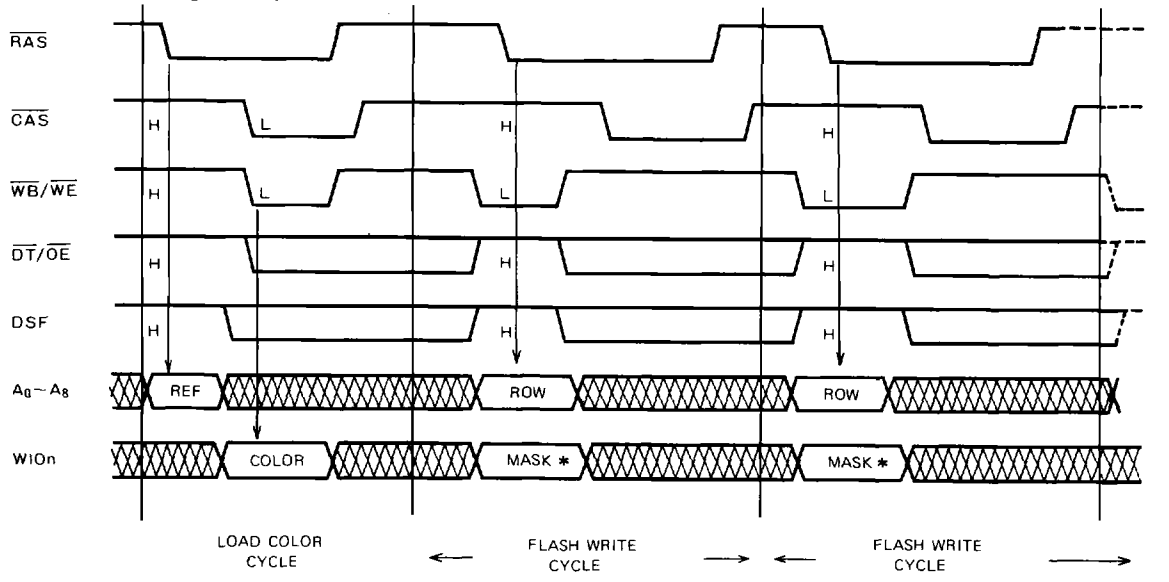
1. Flash Write

Utility: A high speed clear can be performed with flash write cycle.



* Write a color (0 or 1) to an entire row in one RAM cycle.
* Before flash write cycle, the color data must be set into an internal color register at least once.

Flash Write Timing Description

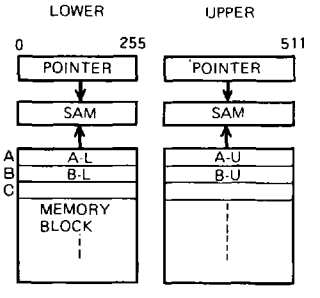


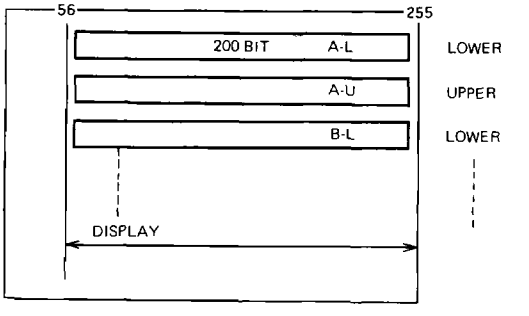
* The mask must be asserted on each flash write cycle.

2. Split Register

Utility

a. To simplify real time transfer timing (Fully asynchronous Serial Access)
b. Split Serial Register into two halves — To optimize the memory size to CRT.

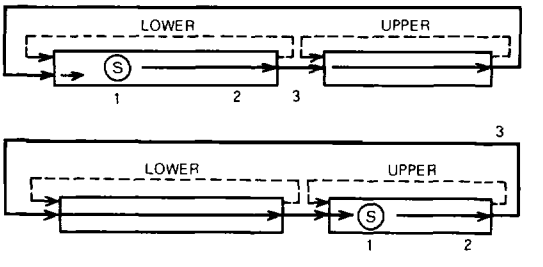




Pointer Path

At Normal read transfer cycle

1. Transfer the data from RAM to SAM, and set the SAM start address among 512.
2. Start the Serial Read cycle.
3. Serial Read from Lower to Upper/Upper to Lower. (The pointer of the Lower/Upper SAM will be automatically cleared to address 0/256 after over-carried)



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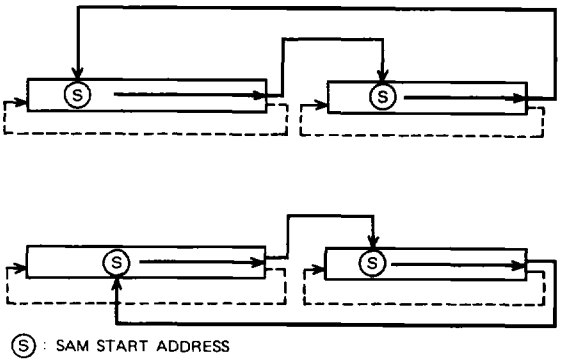
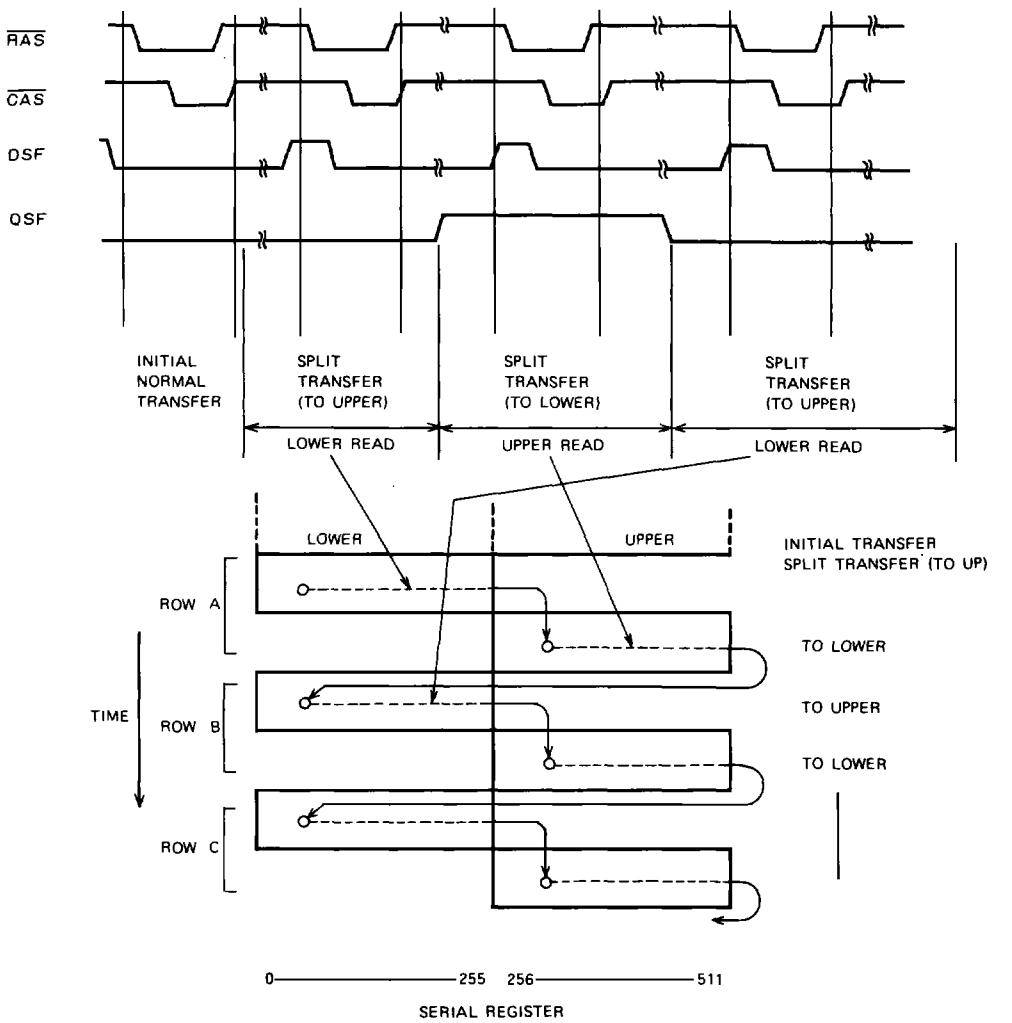
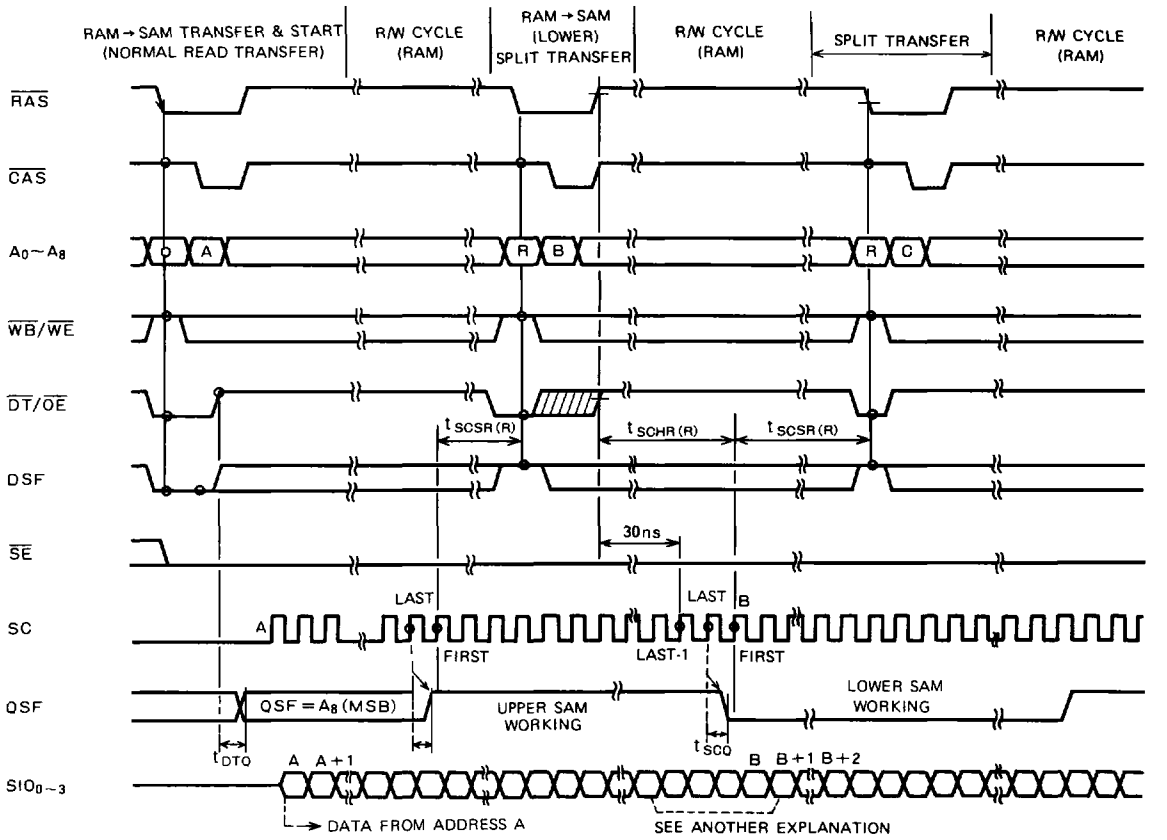
At Split read transfer cycle

1. Normal transfer cycle must be performed prior to the split transfer cycle.
2. The data is transfered between idle half of the SAM and the selected Row. At the same time the idle SAM's start address is set to give the next start address after the end of the busy SAM.
3. At the split transfer mode, data are transfered to the idle half of the SAM automatically. (Column A_8 is ignored.)
4. QSF indicates the busy SAM.
   (Lower Half SAM is busy: 0,
   (Upper Half SAM is busy: 1)
5. Serial Read can be performed asynchronously during RAM cycle and Split transfer cycle.

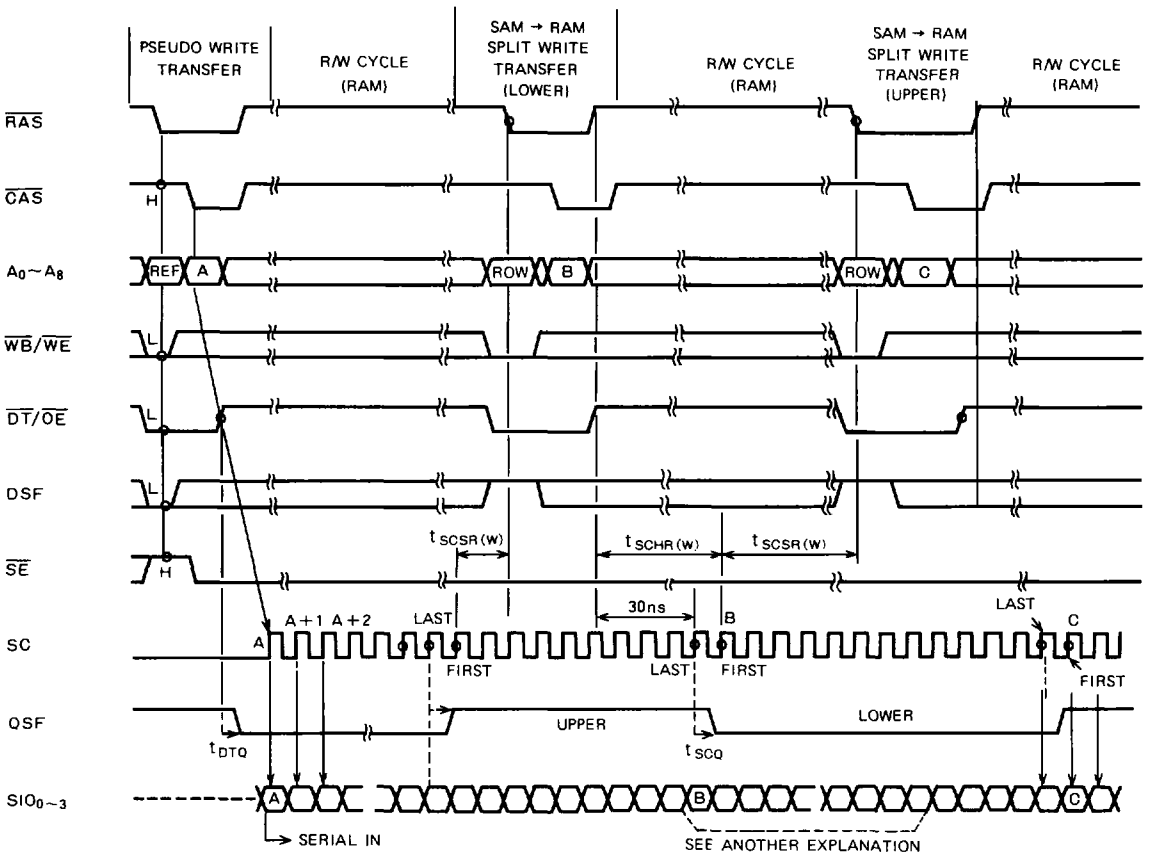




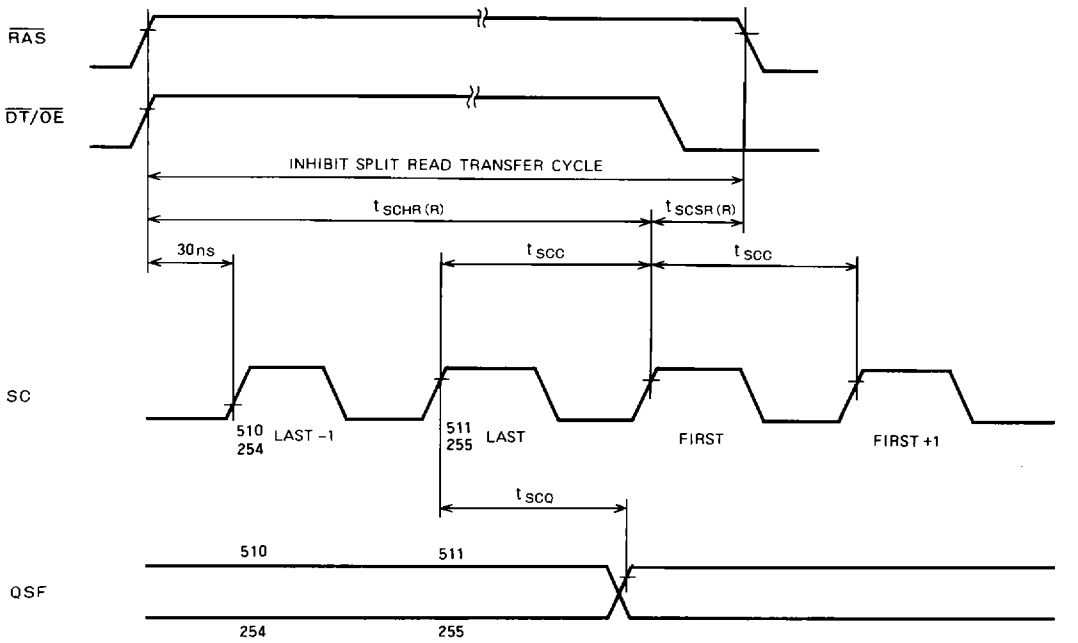
Split Read Transfer Timing Description



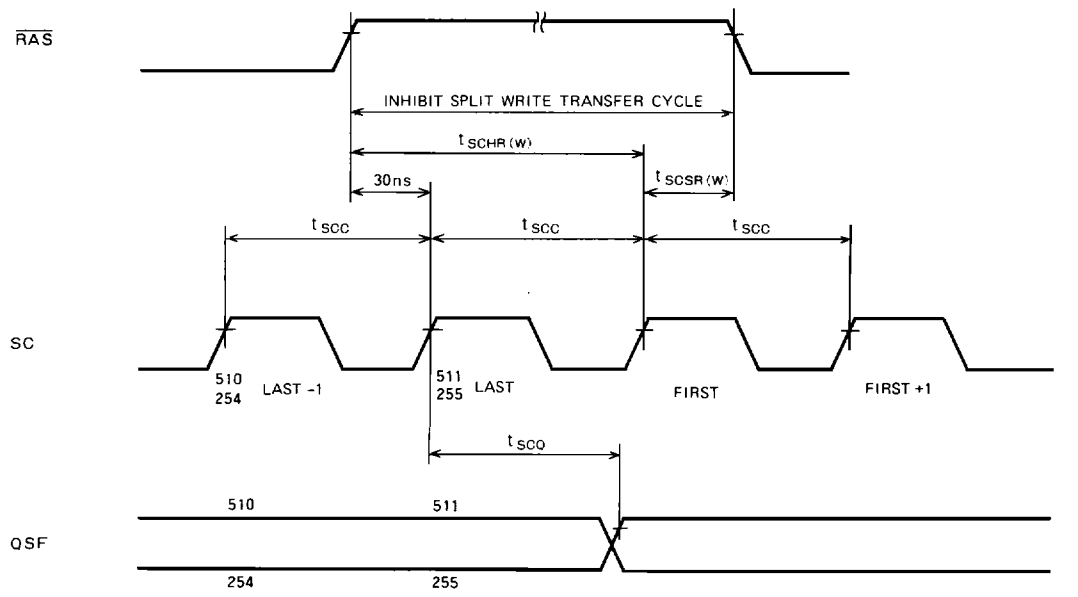
Split Write Transfer Timing Description



Split Read Transfer Inhibit Timing Description

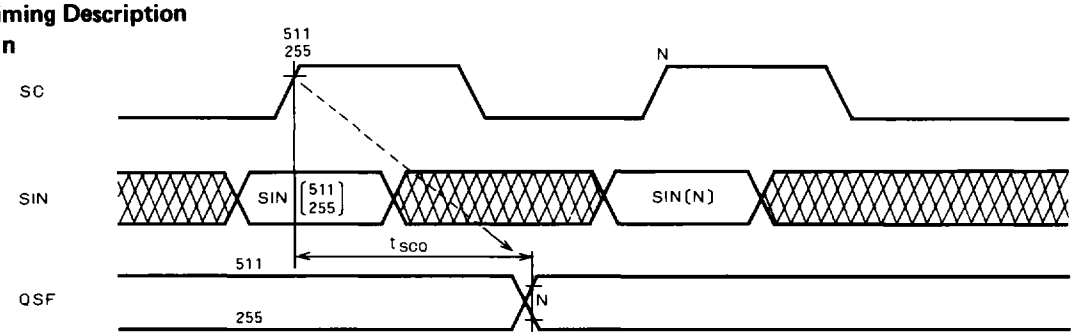


Split Write Transfer Inhibit Timing Description

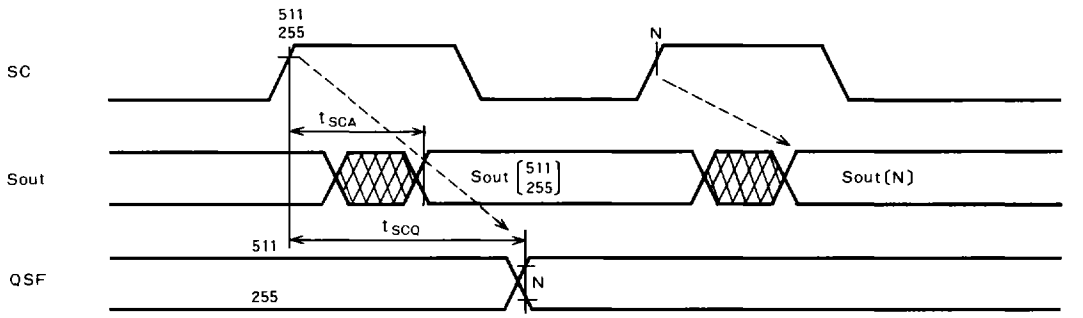


QSF Timing Description

Serial-In



Serial-Out



Data transfer mode	SIO mode	SAM TAP	Data transfer	QSF set
Normal read transfer	Output	Col. (A_0~A_8)	RAM→SAM	A_8
Normal write transfer	Input	Col. (A_0~A_8)	SAM→RAM	A_8
Pseudo write transfer	Input	Col. (A_0~A_8)	—	A_8
Split read transfer	Not effect	Col. (A_0~A_7)	RAM→SAM *1	—
Split write transfer	Not effect	Col. (A_0~A_7)	SAM→RAM *1	—

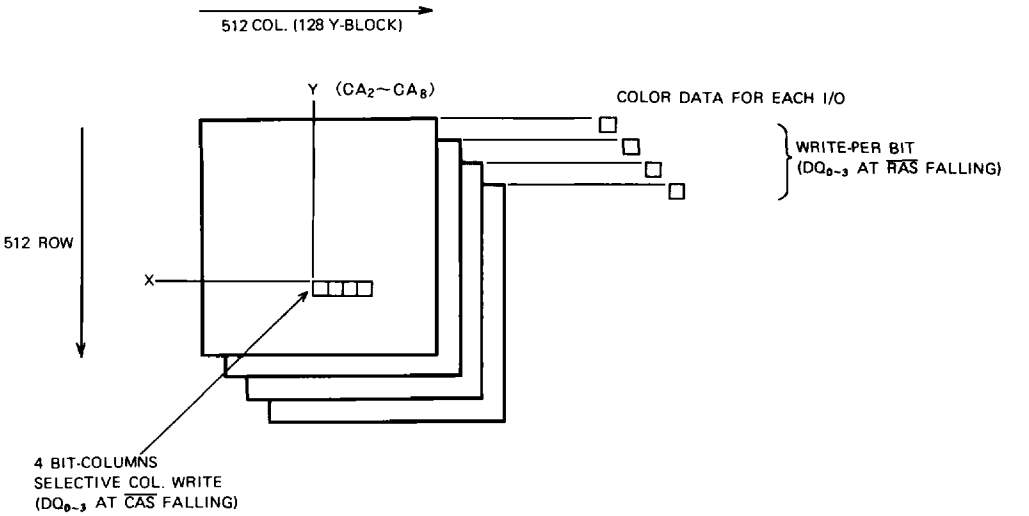
*1: If QSF=0 then the upper half data (256 ~ 511) is transfered.
If QSF=1 then the lower half data (0 ~ 255) is transfered.

3. Block Write

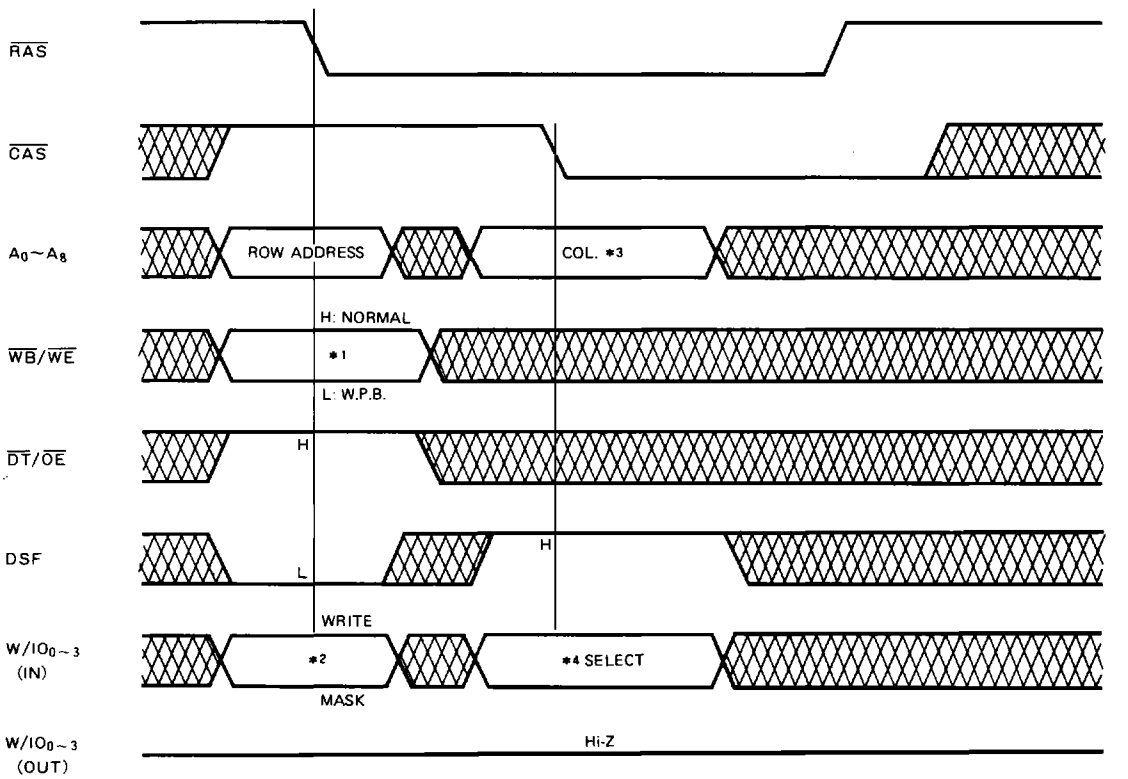
In the Block Write cycle, Data from the Color Register can be written into 4 bit-columns (which Blocks are selected with column address CA_2~CA_8) at one time. The $DQ_{0\sim3}$ the input at $\overline{CAS}$ falling edge enables a selective column write operation of the selected 4 bit-columns.
When $\overline{WB}/\overline{WE}$ is low at $\overline{RAS}$ falling edge Write-per-bit operation applies to the writing of color data.
The Color Register must be loaded prior to the Block Write cycle.

Application

Block Write operation is useful for the partial-clearing or partial-painting of a bit-map display with same color data. With the selective-column writing of data, any of the 4 bit-columns can be masked, so allowing the boundary treatment in the same cycle.



Block Write Timing Description

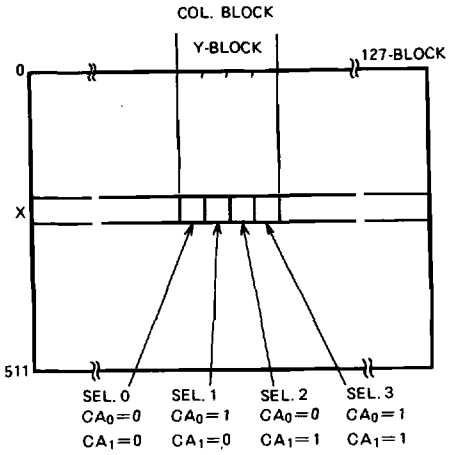


*1: H; No mask
L; Write per bit operation
*2: H; Write enable (No mask)
L; Disable (mask)
*3: Column address $CA_2 \sim CA_8$, CA_0, CA_1 = Don't care (H/L fixed)

Only when $\overline{WB}/\overline{WE}$ is low at $\overline{RAS}$ falling edge

*4. Select
W/IO_0; CA_0=0, CA_1=0
W/IO_1; CA_0=1, CA_1=0
W/IO_2; CA_0=0, CA_1=1
W/IO_3; CA_0=1, CA_1=1

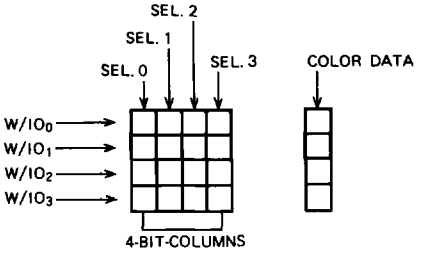
H; Write enable (no mask)
L; Disable (mask)



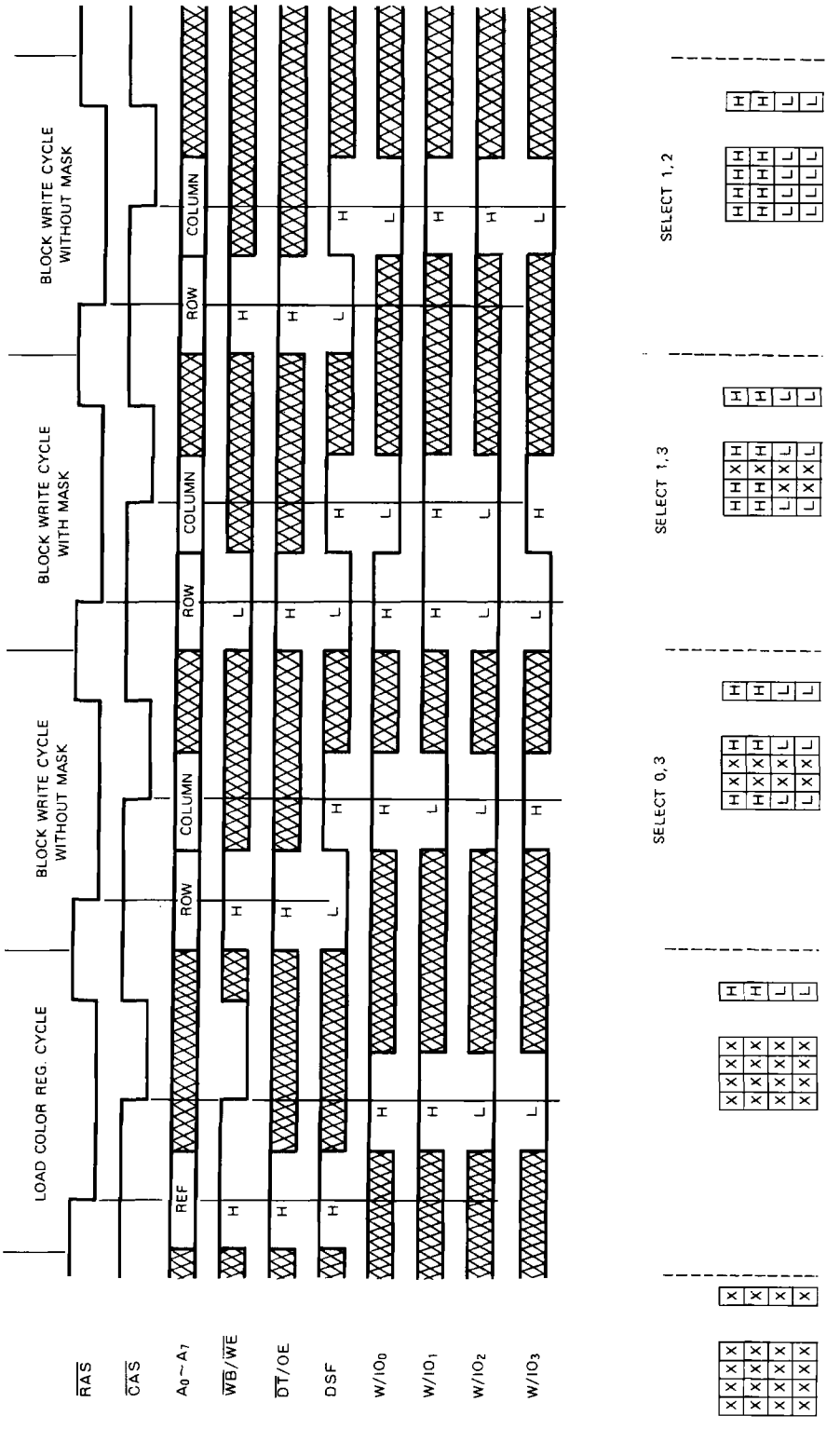
A_0, A_1 at $\overline{CAS}$ falling edge are "don't care", but must be set H or L state.

Example of Block Write Operation

'X' indicates pre-state, 'H'; high level (1), 'L'; low level (0).



Example



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input	2.4		6.5	V
V_{IL}	Low-level input	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(R)}$	High level output (RAM port)	$I_{OH(R)}=-2mA$	2.4		V_{CC}	V
$V_{OL(R)}$	Low level output (RAM port)	$I_{OL(R)}=4.2mA$	0		0.4	V
$V_{OH(S)}$	High level output (Serial I_O port)	$I_{OH(S)}=-2mA$	2.4		V_{CC}	V
$V_{OL(S)}$	Low level output (Serial I_O port)	$I_{OL(S)}=4.2mA$	0		0.4	V
I_{OZ}	Off-state output current	Q Floating $0<V_{out}<V_{CC}$	−10		10	μA
I_I	Input current	$0<V_{in}<V_{CC}$	−10		10	μA

CAPACITANCE (Ta=25°C, f=1MHz, V_I=25mVmrs)

Symbol	Pin name	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}/\overline{OE}$, DSF	$V_I=V_{SS}$, f=1MHz, V_I=25mVrms			8	pF
C_{IN1}	A_0~A_8				8	pF
C_O	WIO_0~WIO_3, SIO_0~SIO_3, QSF				10	pF

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 3)

Symbol	Parameter		Limits			Unit
			M5M442256-8	M5M442256-10	M5M442256-12	
	RAM port	SAM port	Max	Max	Max	
I_{CC1}	Random R/W cycle $\overline{RAS}/\overline{CAS}$ cycling, t_{RC} = t_{RC} (min)	Standby (SC=V_{IL})	80	70	60	mA
I_{CC2}	Standby $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z	(SC=V_{IL})	5	5	5	mA
I_{CC3}	$\overline{RAS}$ only refresh cycle $\overline{RAS}$ = cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	(SC=V_{IL})	80	70	60	mA
I_{CC4}	Page mode cycle $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min	(SC=V_{IL})	70	60	50	mA
I_{CC5}	$\overline{CAS}$ before $\overline{RAS}$ refresh t_{RC} = t_{RC} (min)	(SC=V_{IL})	80	70	60	mA
I_{CC6}	Data transfer cycle t_{RC} = t_{RC} (min)	(SC=V_{IL})	80	70	60	mA
I_{CC7}	Random R/W cycle $\overline{RAS}/\overline{CAS}$ cycling, t_{RC} = t_{RC} (min)	Active (t_{SCC}=min)	140	120	100	mA
I_{CC8}	Standby $\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hi-Z	(t_{SCC}=min)	60	50	40	mA
I_{CC9}	$\overline{RAS}$ only refresh cycle $\overline{RAS}$ = cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	(t_{SCC}=min)	140	120	100	mA
I_{CC10}	Page mode cycle $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{RC} = min	(t_{SCC}=min)	130	110	90	mA
I_{CC11}	$\overline{CAS}$ before $\overline{RAS}$ refresh t_{RC} = t_{RC} min	(t_{SCC}=min)	140	120	100	mA
I_{CC12}	Data transfer cycle t_{RC} = t_{RC} (min)	(t_{SCC}=min)	140	120	100	mA

Note 3. I_{CC} is obtained with the output open.

4. If $V_{IH} \geqq V_{CC} \times 0.9$ and $V_{IL} \leqq 0.6V$.
Then $I_{CC2} \leqq 2.0mA$. ($\overline{DSF}$, $\overline{SE}$ and $SIO_0 \sim SIO_7$ must be stable in high or low level.)

SWITCH CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			M5M442256-8		M5M442256-10		M5M442256-12		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		25		30		35	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		80		100		120	ns
t_{CAA}	Column address access time	(Note 6, 9)		40		50		60	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		45		55		65	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		25		30		35	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	0	30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	20	0	25	0	30	ns
t_{SCA}	Access time from SC high	(Note 6-S)		30		30		40	ns
t_{SOA}	Access time from $\overline{SE}$ low	(Note 6-S)	0	25	0	25	0	35	ns
t_{SOZ}	Output disable time after $\overline{SE}$ high	(Note 11)	0	20	0	20	0	25	ns
t_{SOH}	Serial outut hold time after SC high		5		5		5		ns
t_{SOO}	Delay time $\overline{SE}$ low to serial setup	(Note 6-S)	0		0		0		ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles and 8 SC cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 1TTL loads and 100pF.

6-S: Measured with a load circuit equivalent to 1TTL loads and 30pF.

7: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{RAD(max)} \geqq t_{RAD}$.

8: Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.

9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.

10. Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

11. $t_{OFF(max)}$, $t_{SOZ(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leqq 10\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

Read, Write, Refresh, Read/Write Transfer, Flash Write, Load Color and Fast Page Cycles

Symbol	Parameter		Limits						Unit
			M5M442256-8		M5M442256-10		M5M442256-12		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		70		80		90		ns
t_{RCD}	Delay time $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	30	55	30	70	30	85	ns
t_{CRP}	Delay time $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 16)	35		35		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$	(Note 17)	20	40	20	50	20	60	ns
t_{ASR}	Row address setup time before $\overline{RAS}$		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$	(Note 18)	5	10	5	15	5	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$		15		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		20		20		20		ns
t_T	Transition time	(Note 19)	3	35	3	35	3	35	ns
t_{WSR}	$\overline{WB}/\overline{WE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{RWH}	$\overline{WB}/\overline{WE}$ hold time after $\overline{RAS}$		15		15		15		ns
t_{DTRS}	$\overline{DT}/\overline{OE}$ setup time before $\overline{RAS}$		0		0		0		ns
t_{DTRH}	$\overline{DT}/\overline{OE}$ hold time after $\overline{RAS}$		15		15		15		ns
t_{FSR}	DSF setup time before $\overline{RAS}$		0		0		0		ns
t_{RFH}	DSF hold time after $\overline{RAS}$		15		15		15		ns
t_{FSC}	DSF setup time before $\overline{CAS}$		0		0		0		ns
t_{CFH}	DSF hold time after $\overline{CAS}$		20		20		20		ns
t_{WS}	Write mask setup time before $\overline{RAS}$		0		0		0		ns
t_{WH}	Write mask hold time after $\overline{RAS}$		15		15		15		ns

Note 12: The timing requirements are assumed t_T = 5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only.
If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}.
If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 7, 9.

15: t_{CRP} requirement is applicable for all RAS/CAS cycles.

16: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for t_{CP} of fast page mode cycle.

17: $t_{RAD(max)}$ is specified as a reference point only.
If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.

18: $t_{ASC(max)}$ is specified as a reference point only of address access time.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Max	Min	Min	Max	Min	Max	
t_{RC}	Read cycle time	160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	35	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$	80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	25		30		35		ns
t_{RCS}	Read setup time before $\overline{CAS}$	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	40		50		60		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	25		30		35		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	80		100		120		ns
t_{DOEL}	Delay time date to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to Data	15		20		25		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	25		30		35		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	25		30		35		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Eary Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	160		190		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	25	10000	30	10000	35	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$	80		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	25		30		35		ns
t_{WCS}	Write setup time before $\overline{CAS}$ (Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$	15		20		25		ns
t_{CWL}	$\overline{CAS}$ hold time after write	20		25		30		ns
t_{RWL}	$\overline{RAS}$ hold time after write	20		25		30		ns
t_{WP}	Write pulse width	15		20		25		ns
t_{DSC}	Data setup time before $\overline{CAS}$	0		0		0		ns
t_{DSW}	Data setup time before write	0		0		0		ns
t_{DHC}	Data hold time after $\overline{CAS}$	25		30		35		ns
t_{DHW}	Data hold time after write	20		25		30		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data	15		20		25		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write	15		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M442256-8		M5M442256-10		M5M442256-12		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 21)	205		245		285		ns
t_{RAS}	$\overline{RAS}$ low pulse width		125	10000	155	10000	185	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		70	10000	85	10000	100	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$		125		155		185		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		70		85		100		ns
t_{RCS}	Read setup time before $\overline{CAS}$		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write	(Note 22)	45		55		65		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write	(Note 22)	100		125		150		ns
t_{CWL}	$\overline{CAS}$ hold time after write		20		25		30		ns
t_{RWL}	$\overline{RAS}$ hold time after write		20		25		30		ns
t_{WP}	Write pulse width		15		20		25		ns
t_{DSW}	Data setup time before write		0		0		0		ns
t_{DHW}	Data hold time after write		20		25		30		ns
t_{AWD}	Delay time address to write	(Note 22)	60		75		90		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$		25		30		35		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$		80		100		120		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		0		0		0		ns
t_{DEHD}	Delay time, $\overline{OE}$ high to data		15		20		25		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low		15		20		25		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only.
If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the WIO pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{RWD} \geq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the WIO will contain the data read from the selected address.
If neither of the above conditions is satisfied, the condition of the WIO (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter		Limits						Unit
			M5M442256-8		M5M442256-10		M5M442256-12		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Read, write cycle time		50		60		70		ns
t_{RWPC}	Read, write/read modify write cycle time		100		115		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle		135	100k	160	100k	190	100k	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle		25	10000	30	10000	35	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 23)	10	15	10	20	15	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$		25		30		35		ns

Note 23: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	30		35		40		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 24: Eight of more $\overline{CAS}$ before $\overline{RAS}$ cycle is nesessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Normal Read/Write/Pseudo Write Transfer

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
t_{RDH} *	$\overline{DT}/\overline{OE}$ low hold time after $\overline{RAS}$	70		80		90		ns
t_{RSD}	Delay time $\overline{RAS}$ to SC	90		105		120		ns
t_{ASD}	Delay time address to SC	55		60		65		ns
t_{CSD}	Delay time $\overline{CAS}$ to SC	50		55		60		ns
t_{SDH}	SC hold time after $\overline{DT}$	15		15		20		ns
t_{RQ}	Delay time $\overline{RAS}$ to QSF		105		125		140	ns
t_{AQ}	Delay time address to QSF		70		80		85	ns
t_{CQ}	Delay time $\overline{CAS}$ to QSF		75		85		90	ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF		30		35		40	ns
t_{DTSR}	$\overline{DT}$ high setup time before $\overline{RAS}$ high (Note 25)	0		0		0		ns
t_{DTW}	$\overline{DT}$ high pulse width	20		25		30		ns
t_{ES}	$\overline{SE}$ setup time before $\overline{RAS}$ low	0		0		0		ns
t_{EH}	$\overline{SE}$ hold time after $\overline{RAS}$ low	15		15		15		ns
t_{SZR}	$\overline{RAS}$ low to serial input delay time (Serial-in → Serial-out)	20		20		20		ns
t_{RLZ}	$\overline{RAS}$ to serial output delay time (Serial-out → Serial-in)	25		25		25		ns
t_{SRS}	SC setup time before $\overline{RAS}$ low	30		35		40		ns
t_{SDZ}	Serial output turn-off delay time (Serial-out → Serial-in)	10	50	10	50	10	60	ns
t_{SDP}	$\overline{RAS}$ to Serial input delay time (Serial-out → Serial-in)	50		50		60		ns

* If $t_{RCD} \geqq 70$ns, $t_{RDH(min)}$ is 15ns.

$\overline{RAS}$ Control Read/Write/Pseudo Write Transfer

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
t_{RDTD}	$\overline{DT}$ hold time after $\overline{RAS}$ high (Note 25)	0		0		0		ns
t_{SRH}	SC hold time after $\overline{RAS}$= high	20		20		25		ns
t_{DTW}	$\overline{DT}$ high pulse width	20		25		30		ns
t_{RHQ}	Delay time $\overline{RAS}$ high to QSF		30		30		40	ns
t_{SZSR}	Delay time data to $\overline{RAS}$ high	0		0		0		ns
t_{RHZ}	$\overline{RAS}$ high serial output delay time (Serial-in → Serial-out)	5		5		5		ns

Note 25: $t_{RDTD(min)}$ and $t_{DTSR(min)}$ are specified as a reference point only. If $t_{RDTD} \geqq t_{RDTD(min)}$, the cycle is $\overline{RAS}$ control transfer cycle.

Split Read/Write Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
$t_{SCSR(W)}$	SC setup time to $\overline{RAS}$ at split write transfer cycle	30		30		40		ns
$t_{SCHR(W)}$	SC hold time from $\overline{RAS}$ at split write transfer cycle	t_{SCC} +30		t_{SCC} +30		t_{SCC} +40		ns
$t_{SCSR(R)}$	SC setup time to $\overline{RAS}$ at split read transfer cycle	0		0		0		ns
$t_{SCHR(R)}$	SC hold time from $\overline{RAS}$ at split read transfer cycle	$2t_{SCC}$ +30		$2t_{SCC}$ +30		$2t_{SCC}$ +40		ns

Serial Input/Serial Output

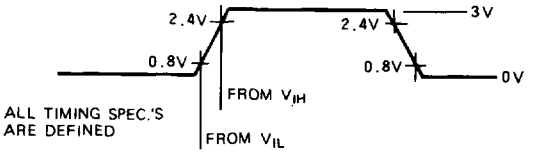
Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
$t_{SCC(R)}$	SC clock cycle time	30		30		40		ns
$t_{SCC(W)}$	SC high pulse width	30		40		40		ns
t_{SCL}	SC low pulse width	10		10		15		ns
t_{SOP}	$\overline{SE}$ high pulse width	25		25		35		ns
t_{SOE}	$\overline{SE}$ low pulse width	25		25		35		ns
t_{SIH}	Serial input data hold time after SC high	20		20		30		ns
t_{SIS}	Serial input data setup time before SC high	0		0		0		ns
t_{SWIH}	$\overline{SE}$ disable hold time after SC high	15		15		20		ns
t_{SWIS}	$\overline{SE}$ disable setup time before SC high	10		10		10		ns
t_{SWH}	$\overline{SE}$ enable hold time after SC high	15		15		20		ns
t_{SWS}	$\overline{SE}$ enable setup time before SC high	10		10		10		ns
t_{SCQ}	Delay time SC to QSF		30		30		40	ns

Read Time Read Transfer

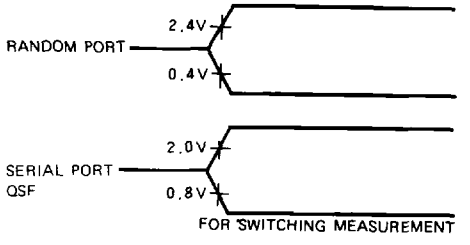
Symbol	Parameter	Limits						Unit
		M5M442256-8		M5M442256-10		M5M442256-12		
		Min	Max	Min	Max	Min	Max	
t_{RDH}	$\overline{DT}$ hold time after $\overline{RAS}$	70		85		100		ns
t_{CDH}	$\overline{DT}$ hold time after $\overline{CAS}$	30		35		40		ns
t_{ADH}	$\overline{DT}$ hold time after address	35		40		45		ns
t_{SDD}	Delay time SC to $\overline{DT}$	20		20		25		ns
t_{SDH}	SC hold time after $\overline{DT}$	30		30		35		ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF (Note 25)		30		30		40	ns
t_{RDTD}	$\overline{DT}$ hold time after $\overline{RAS}$ high	0		0		0		ns
t_{SRD}	Delay time SC to $\overline{RAS}$ high (Note 25)	15		15		20		ns
t_{SRH}	SC hold time after $\overline{RAS}$ high (Note 25)	35		35		40		ns
t_{RHQ}	Delay time $\overline{RAS}$ high to QSF (Note 25)		30		30		40	ns

Switching Measurement Condition

1. Input reference point

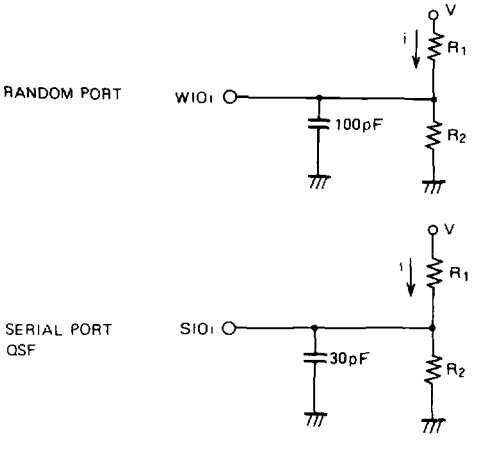


2. Output reference point



DC LEVEL OF OUTPUT IS V_{OH} = 2.4V, V_{OL} = 0.4V

3. Load condition



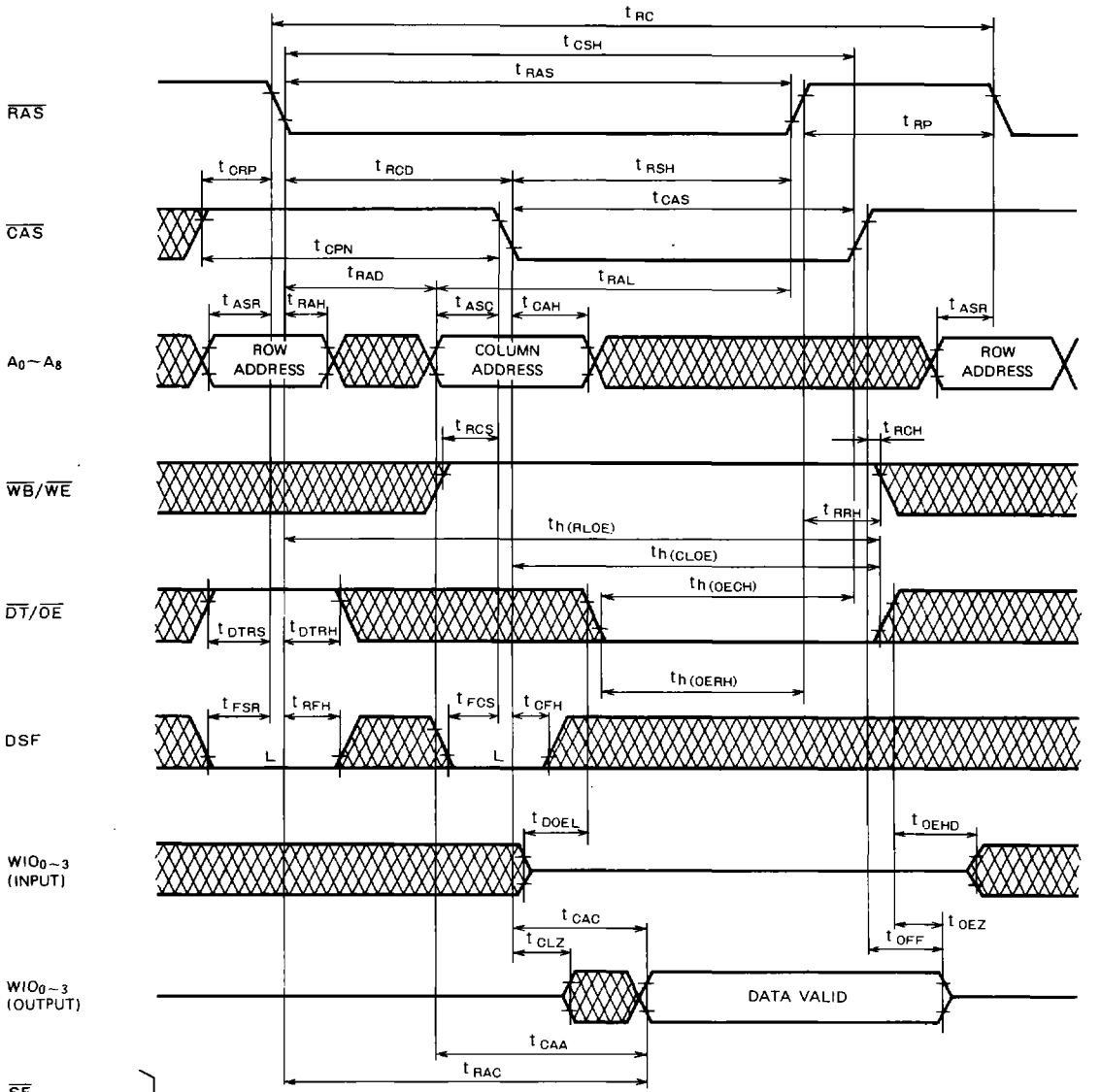
$$\left[\begin{array}{ll} V = V_{OH} + R_1 \cdot I_H & V = V_{OL} + R_1 \cdot I_L \\ V_{OH} = (I_H - I_{OH}) \cdot R_2 & V_{OL} = (I_L - I_{OL}) \cdot R_2 \end{array}\right]$$

When V = 5V, R_1 = 919 Ω, R_2 = 497 Ω

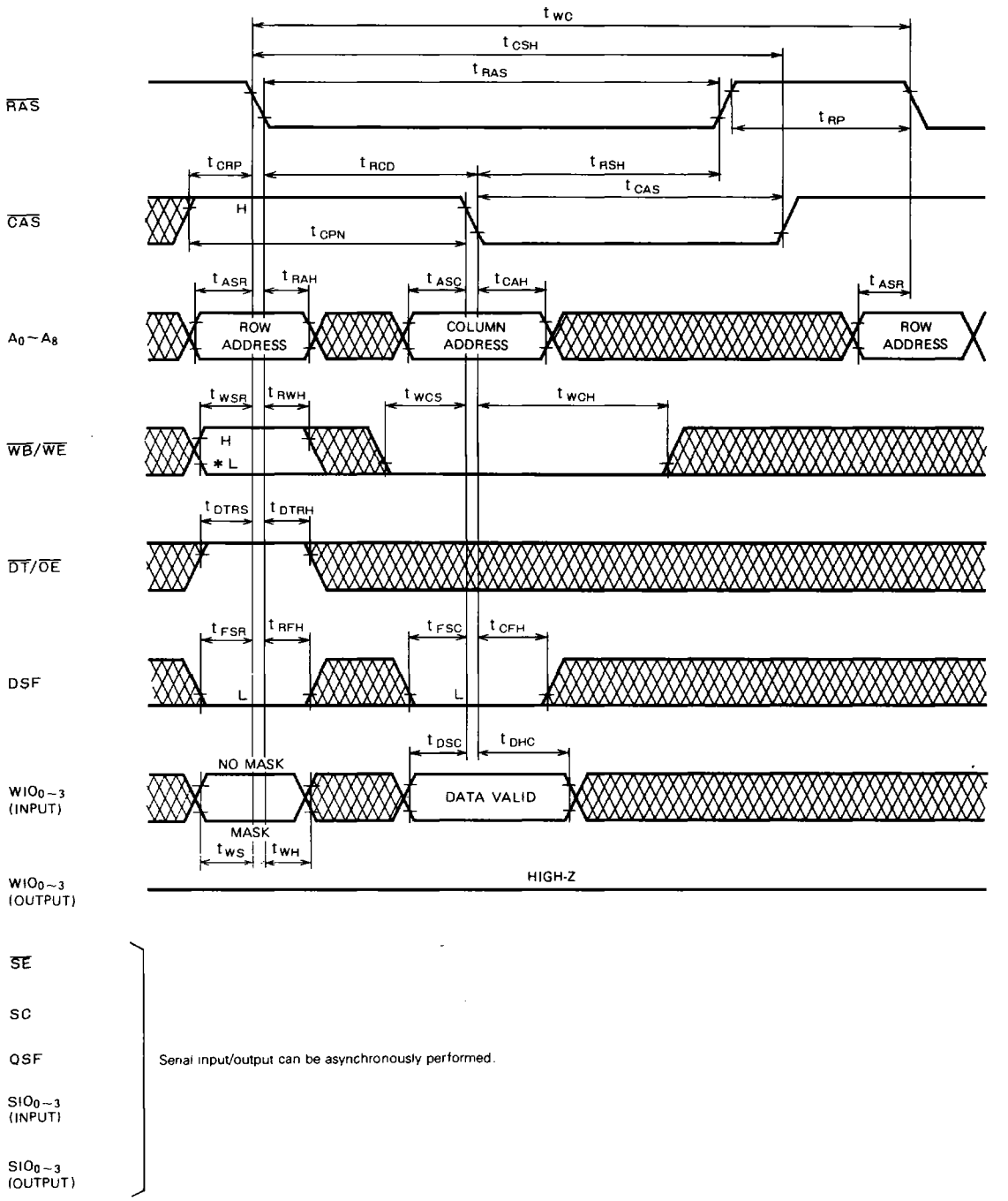
$$\left[\begin{array}{l} R_1 = \dfrac{V_{OH}(V - V_{OL}) - V_{OL}(V - V_{OH})}{V_{OH} \cdot I_{OL} - V_{OL} \cdot I_{OH}} \\ \\ R_2 = \dfrac{V_{OH} \cdot R_1}{(V - V_{OH}) - I_{OH} \cdot R_1} \end{array}\right]$$

TIMING DIAGRAMS

Normal Read Cycle

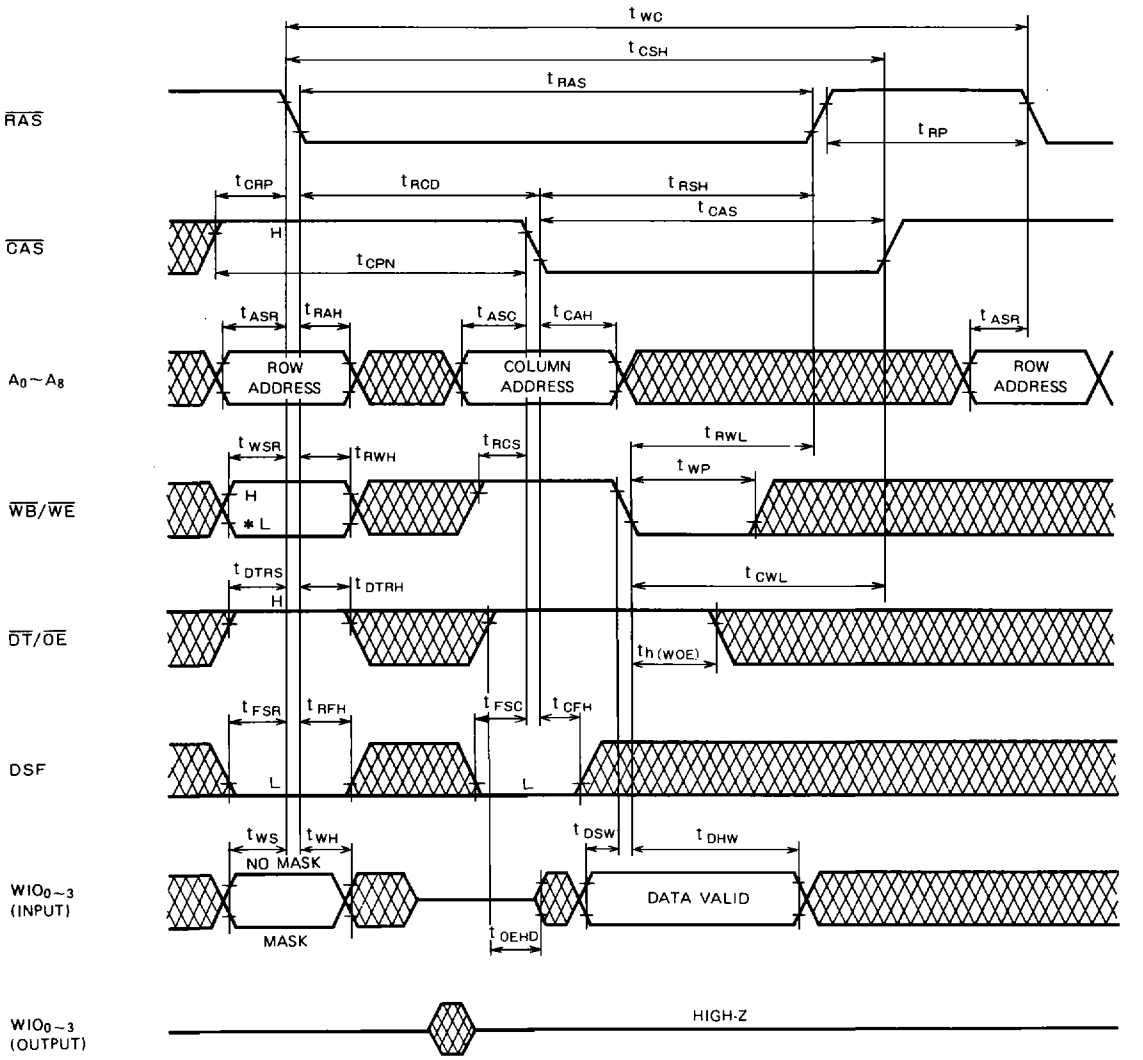


Normal Write Cycle (Early Write)



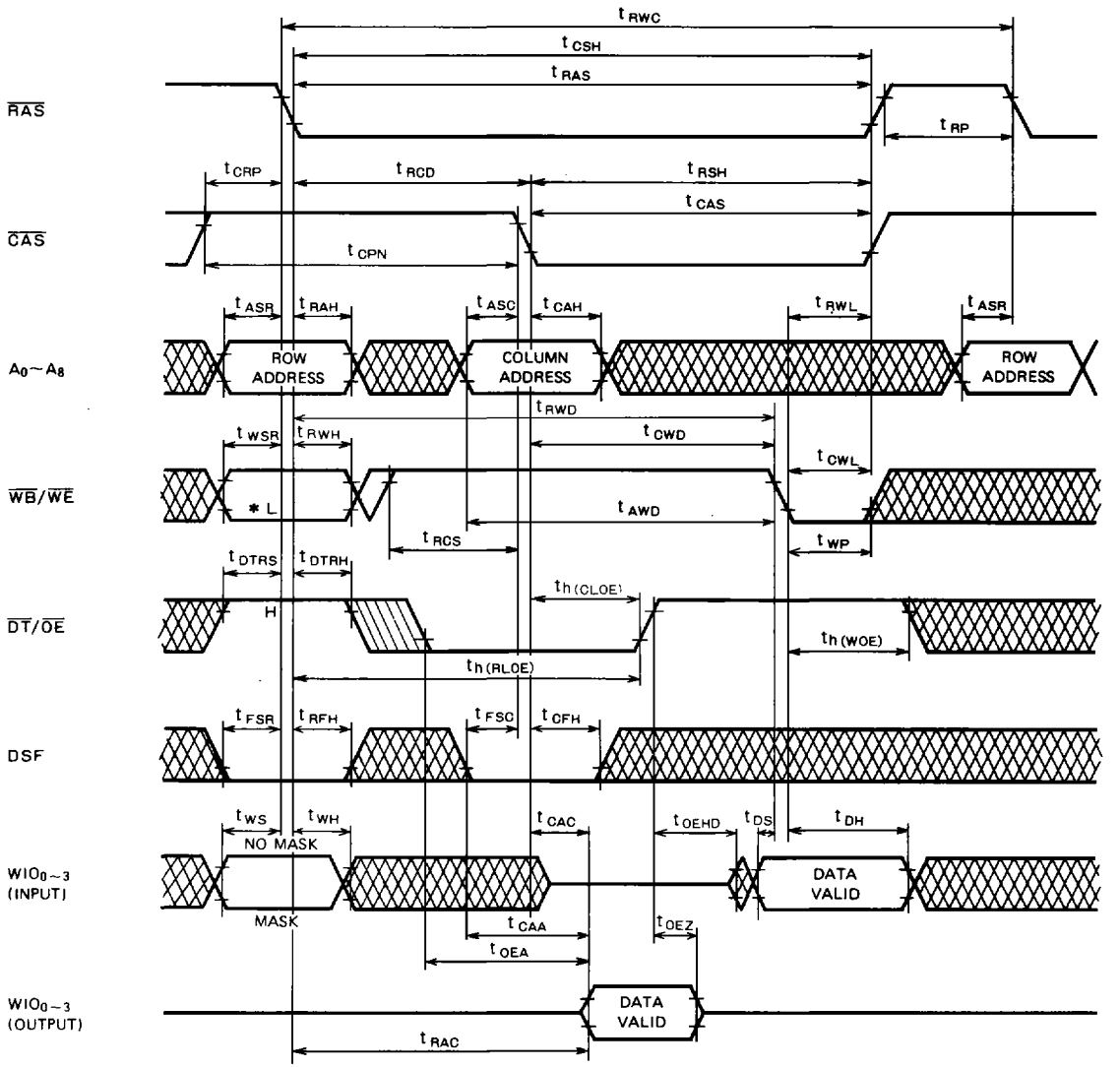
*L = Write per bit operation (New mask)

Normal Write Cycle (Late Write)



*L = Write per bit operation (New mask)

Normal Read Modify Write Cycle



* L = Write per bit operation

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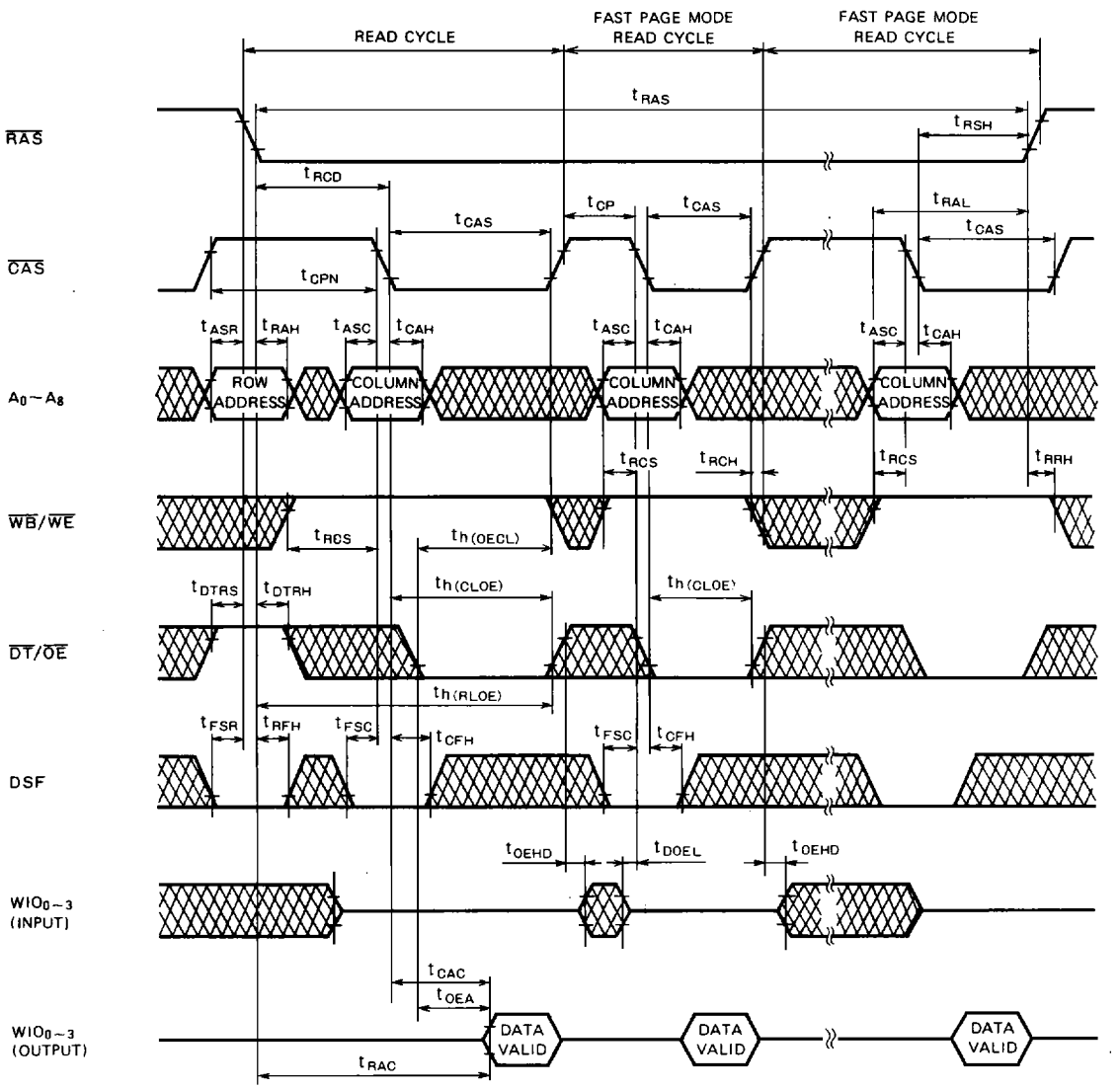
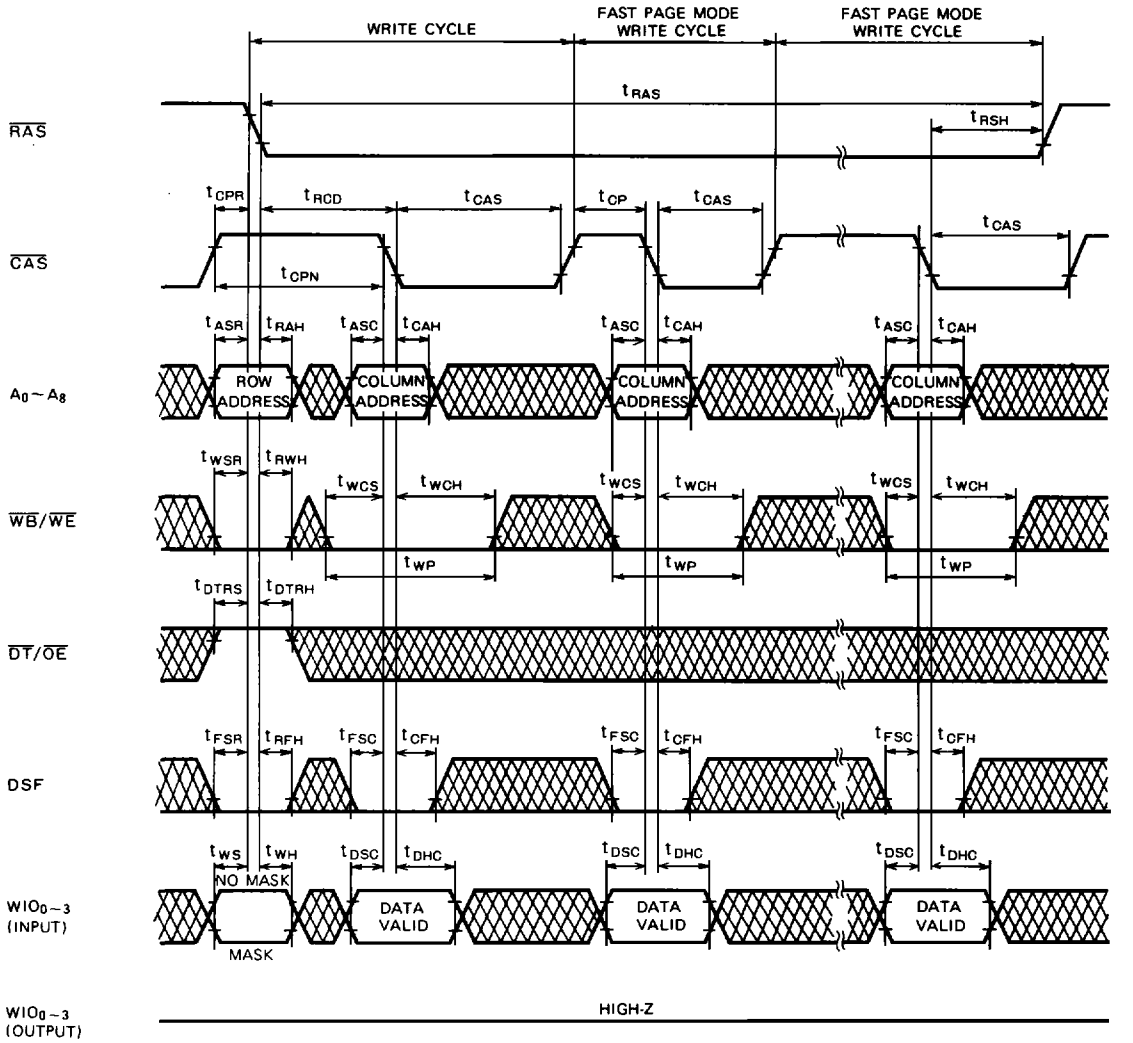
Fast Page Mode Read Cycle



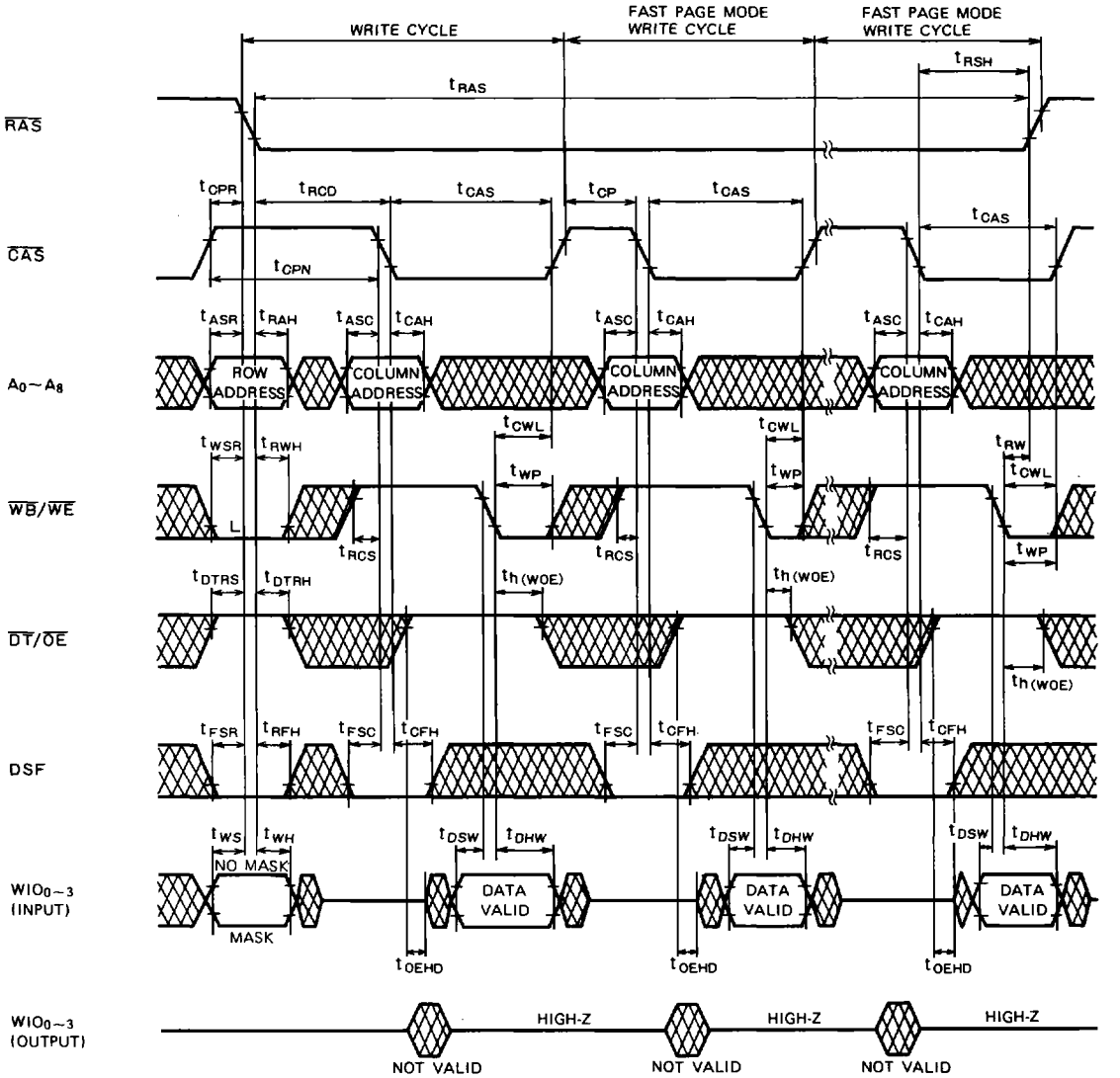
Fast Page Mode Early Write Cycle with New Mask



Serial input/output can be asynchronously performed

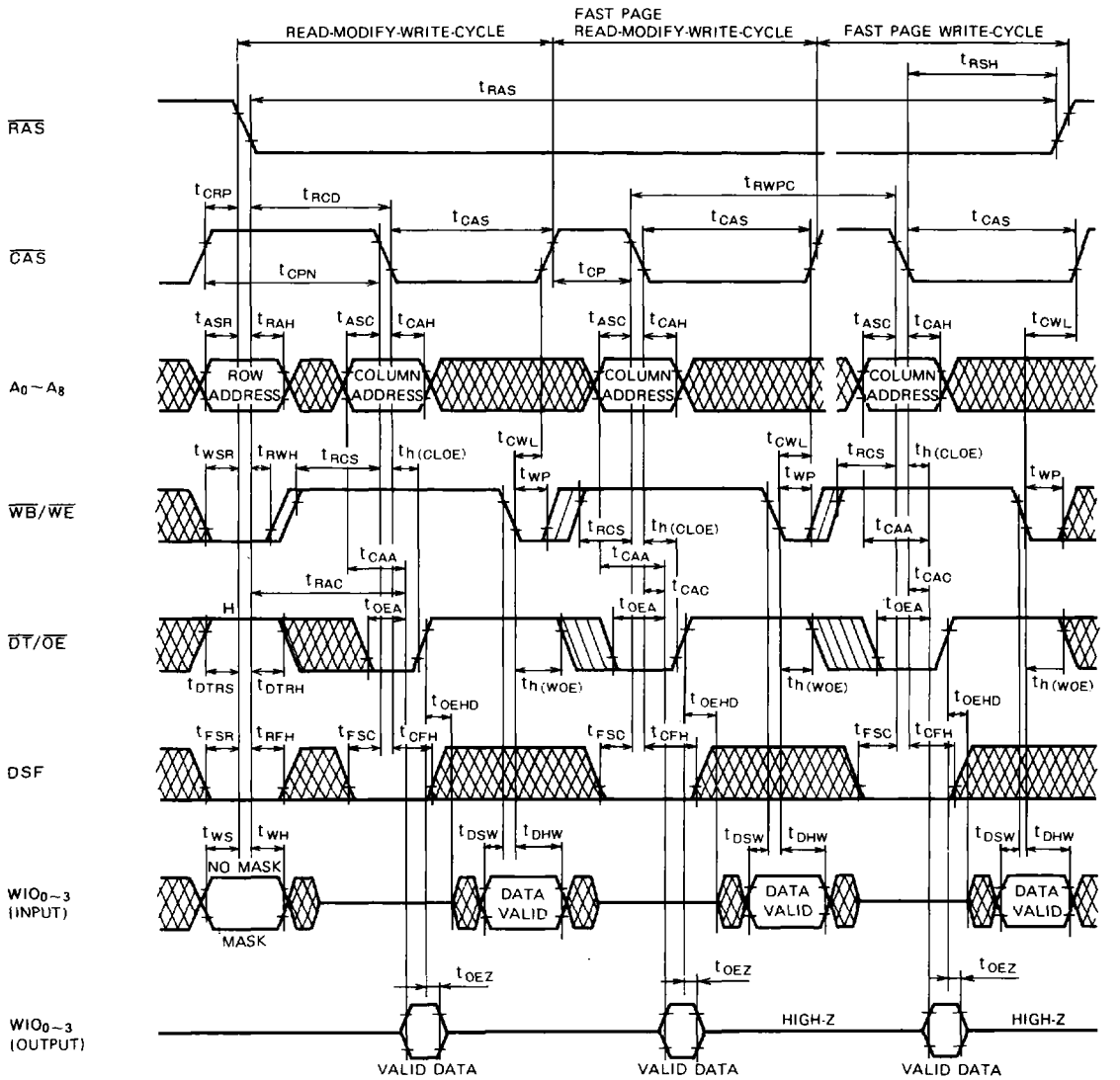
Write per bit operation mask is effective during the continuous page mode cycle.

Fast Page Mode Late Write with New Mask



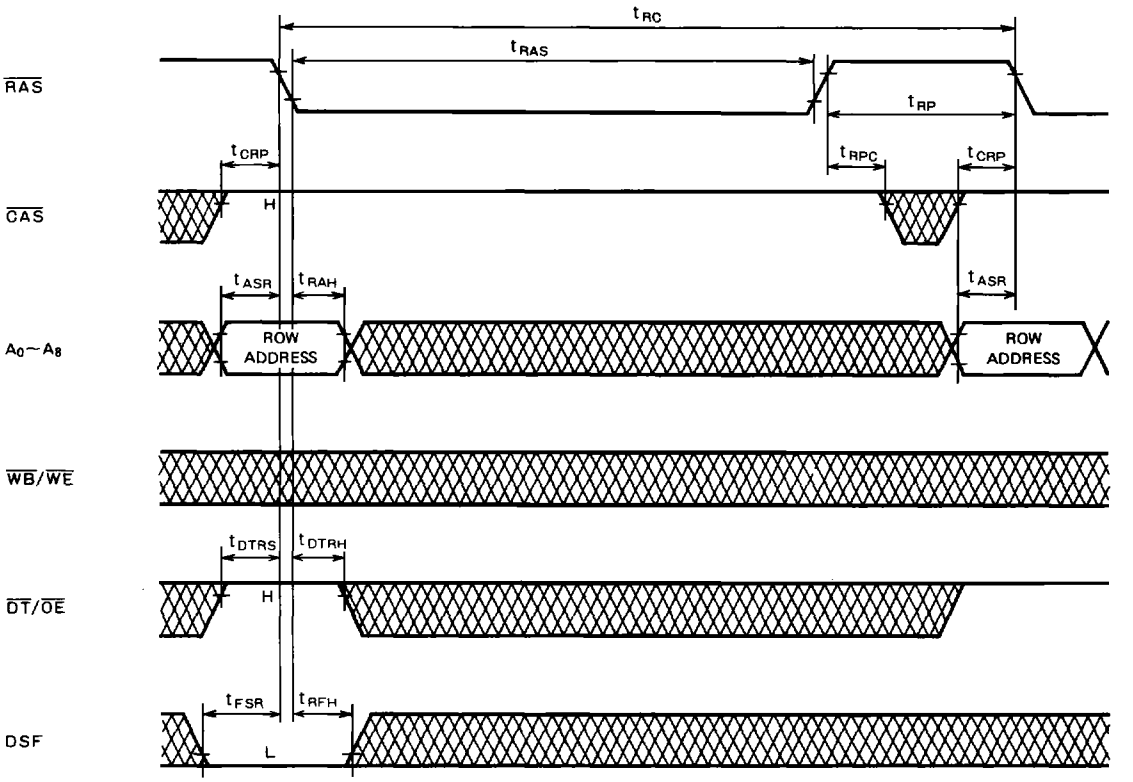
Serial input/output can be asynchronously performed.
Write per bit operation mask is effective during the continuous page mode cycle.

Fast Page Mode Read-Write, Read-Modify-Write-Cycle with New Mask



Serial input/output can be asynchronously performed.
Write per bit operation mask is effective during the continuous page mode cycle.

$\overline{RAS}$ only Refresh Cycle



$\overline{SE}$

SC

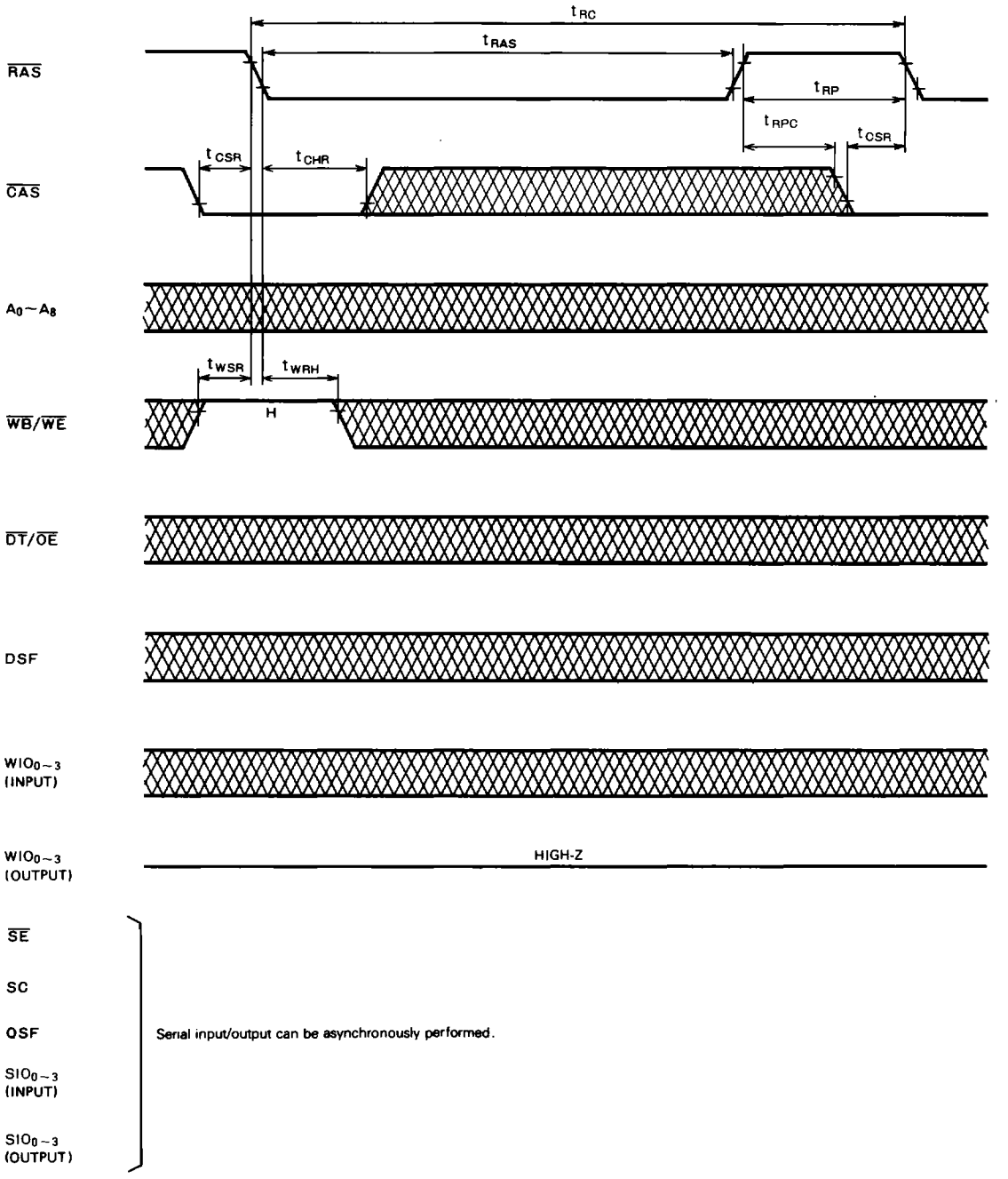
QSF

Serial input/output can be asynchronously performed.

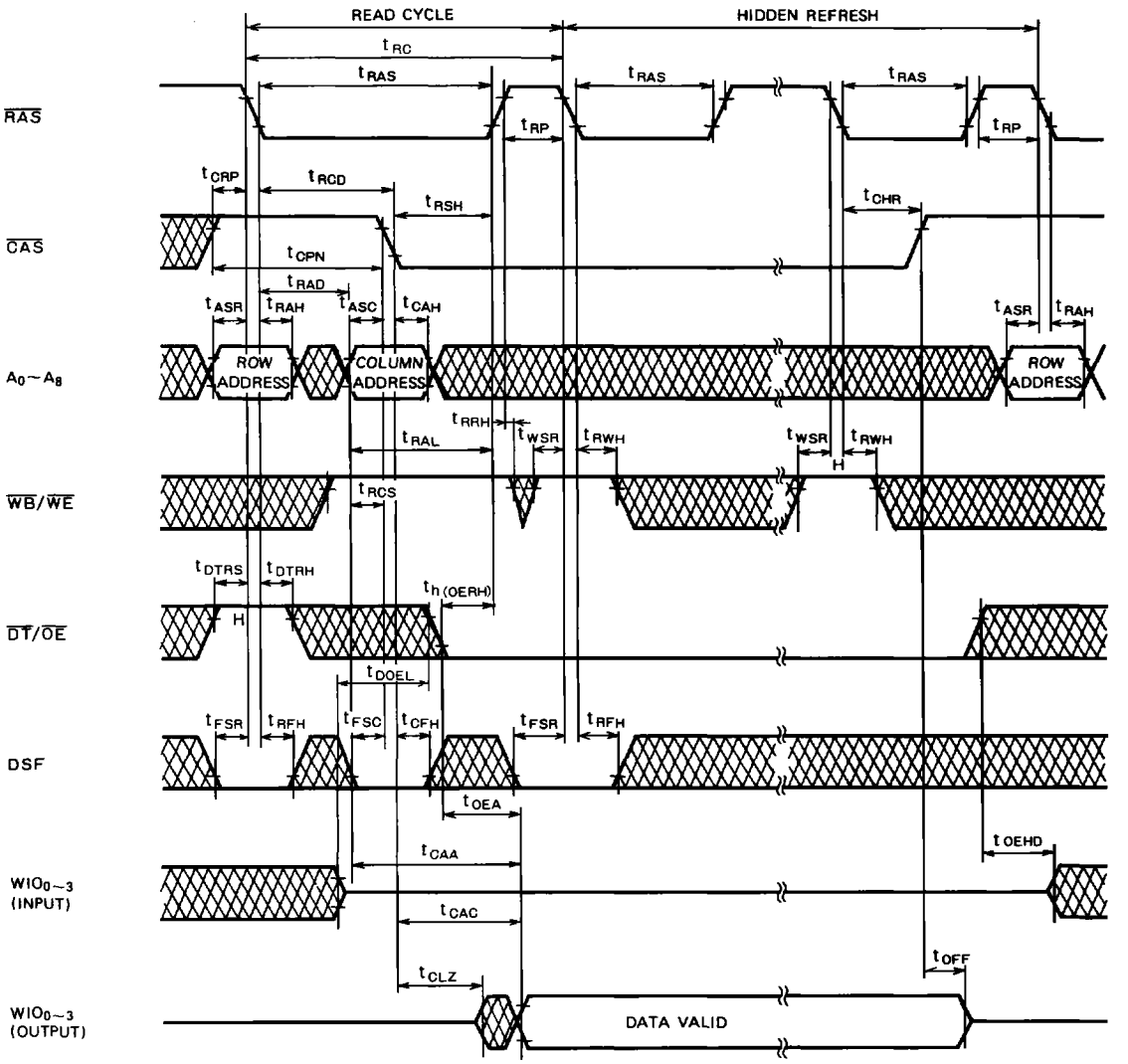
$SIO_{0\sim3}$ (INPUT)

$SIO_{0\sim3}$ (OUTPUT)

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

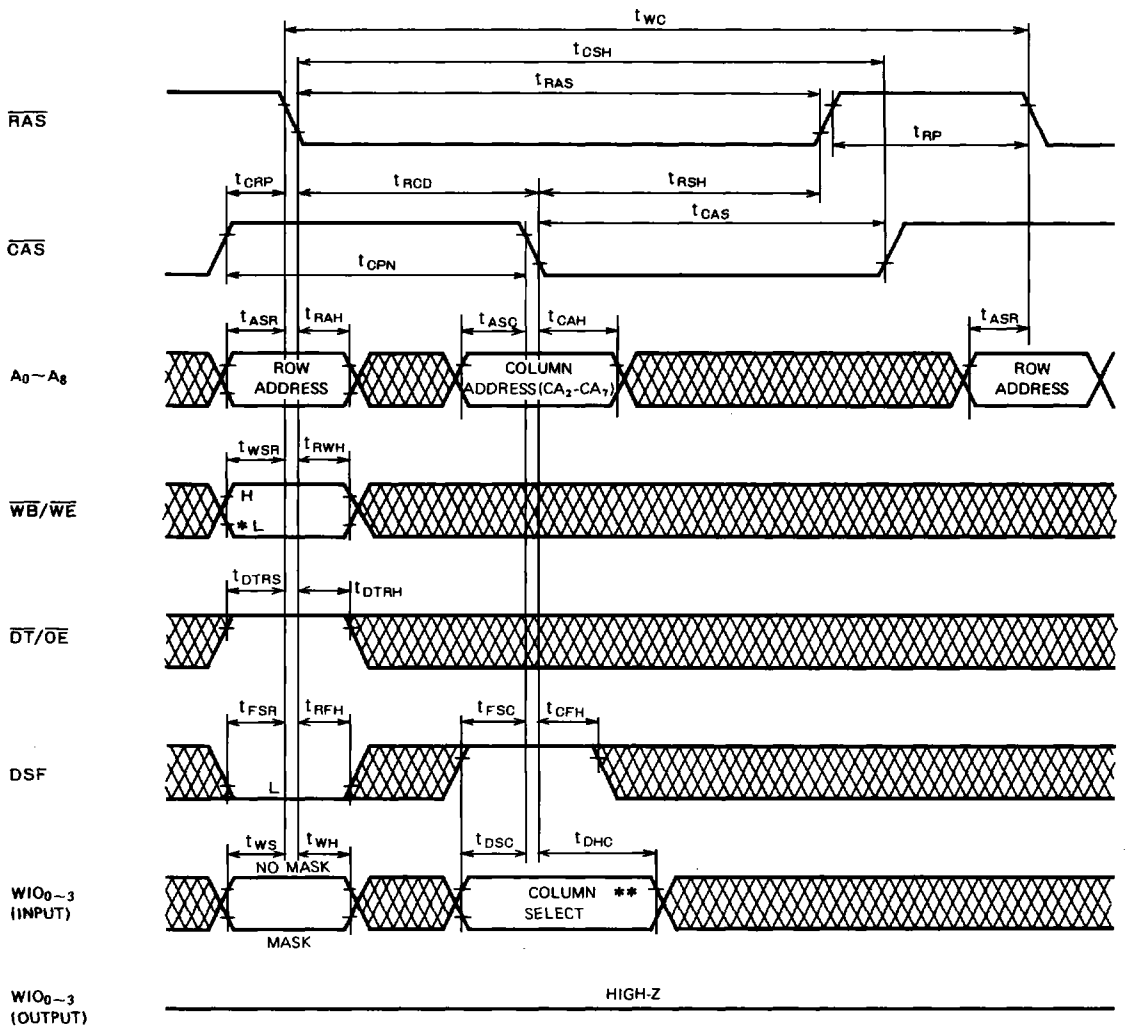


Hidden Refresh Cycle (Automatic Refresh)



Serial input/output can be asynchronously performed.

Block Write Cycle

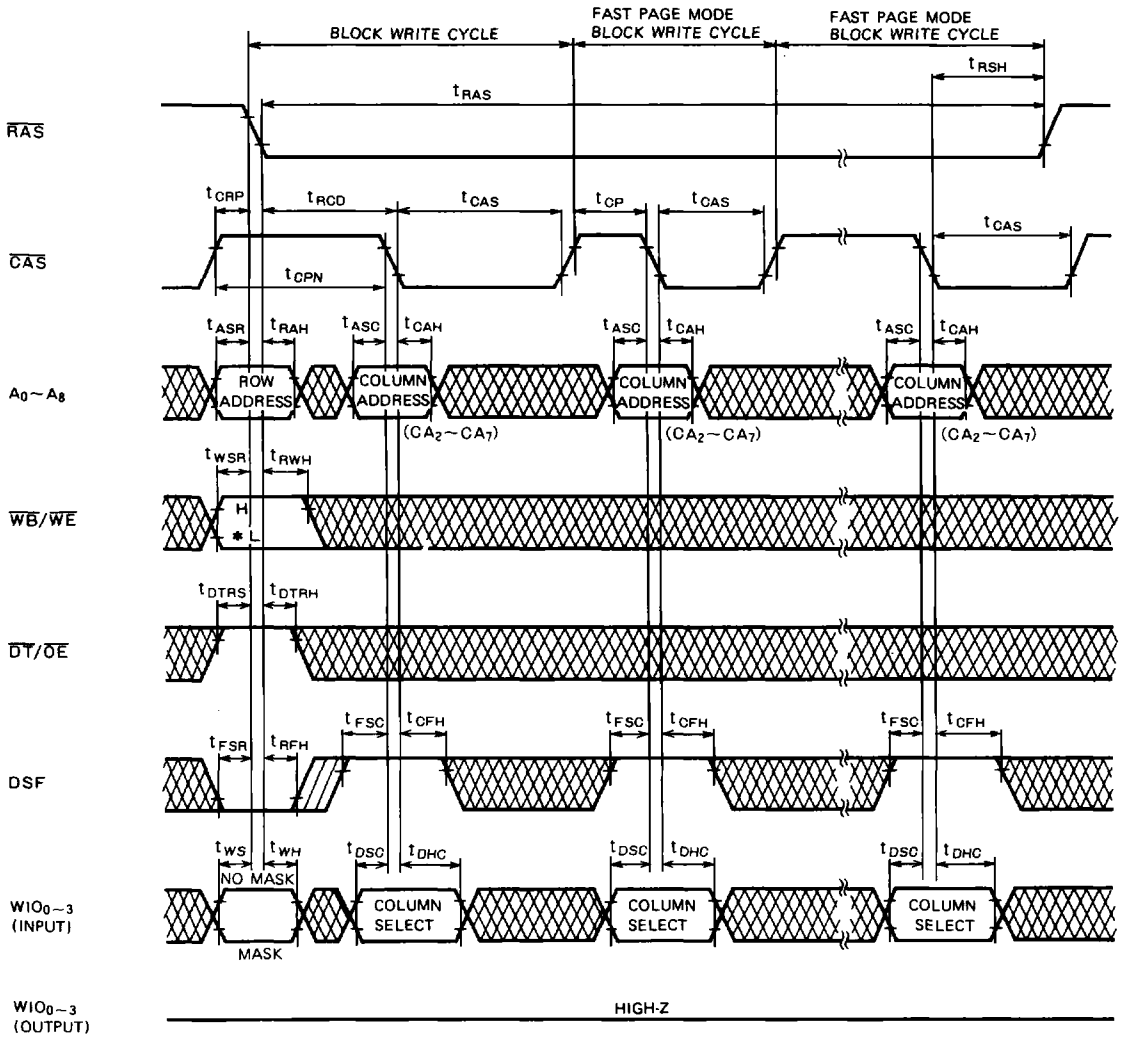


* L = Write per bit (New mask)
Fast page mode can be applied.

** When WIO_n = 1, the Col.-n is selected.

WIO 0 **	···Col-0	$CA_0=0$, $CA_1=0$
1	···Col-1	$CA_0=1$, $CA_1=0$
2	···Col-2	$CA_0=0$, $CA_1=1$
3	···Col-3	$CA_0=1$, $CA_1=1$

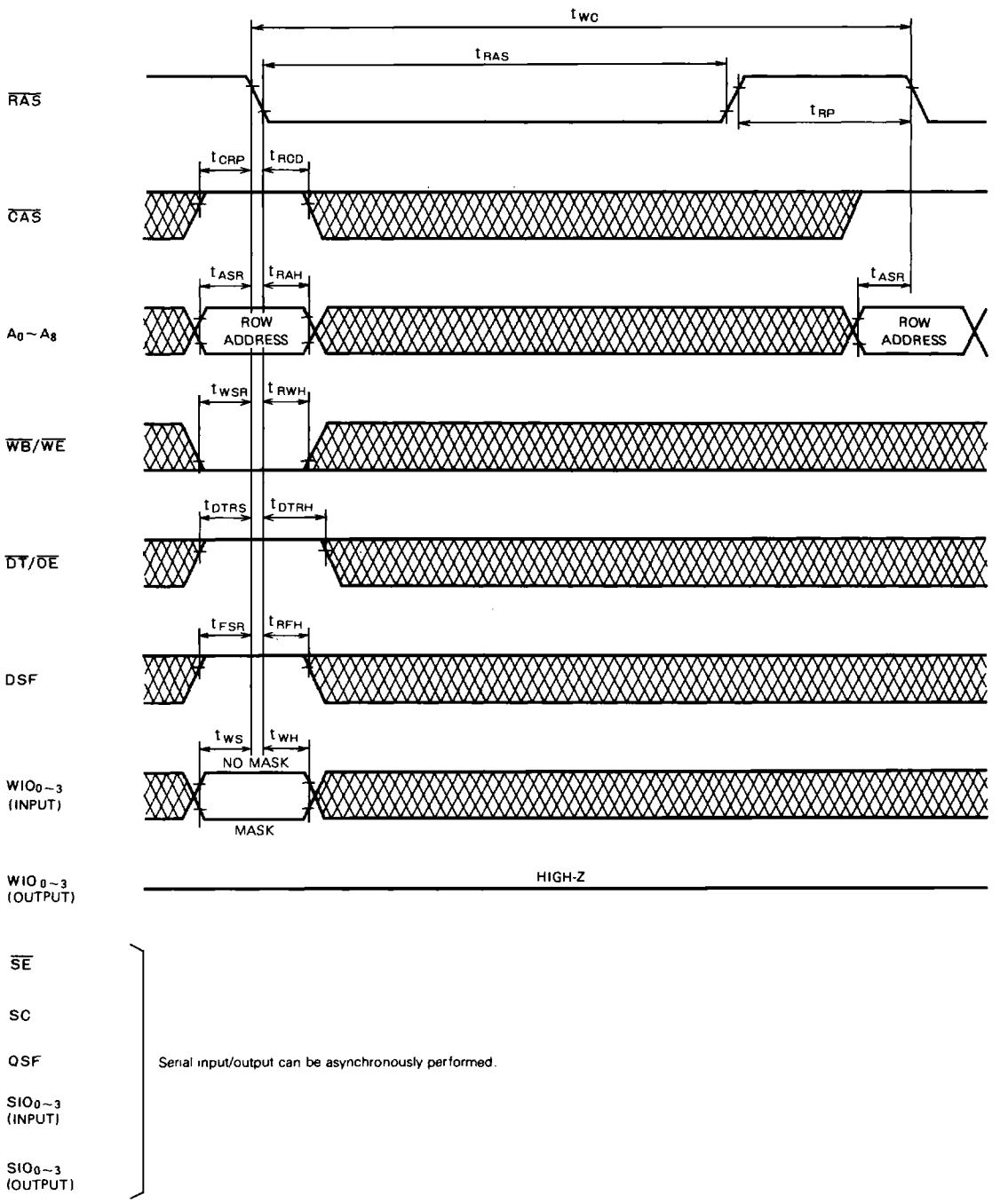
Fast Page Mode Block Write Cycle



Serial input/output can be asynchronously performed.

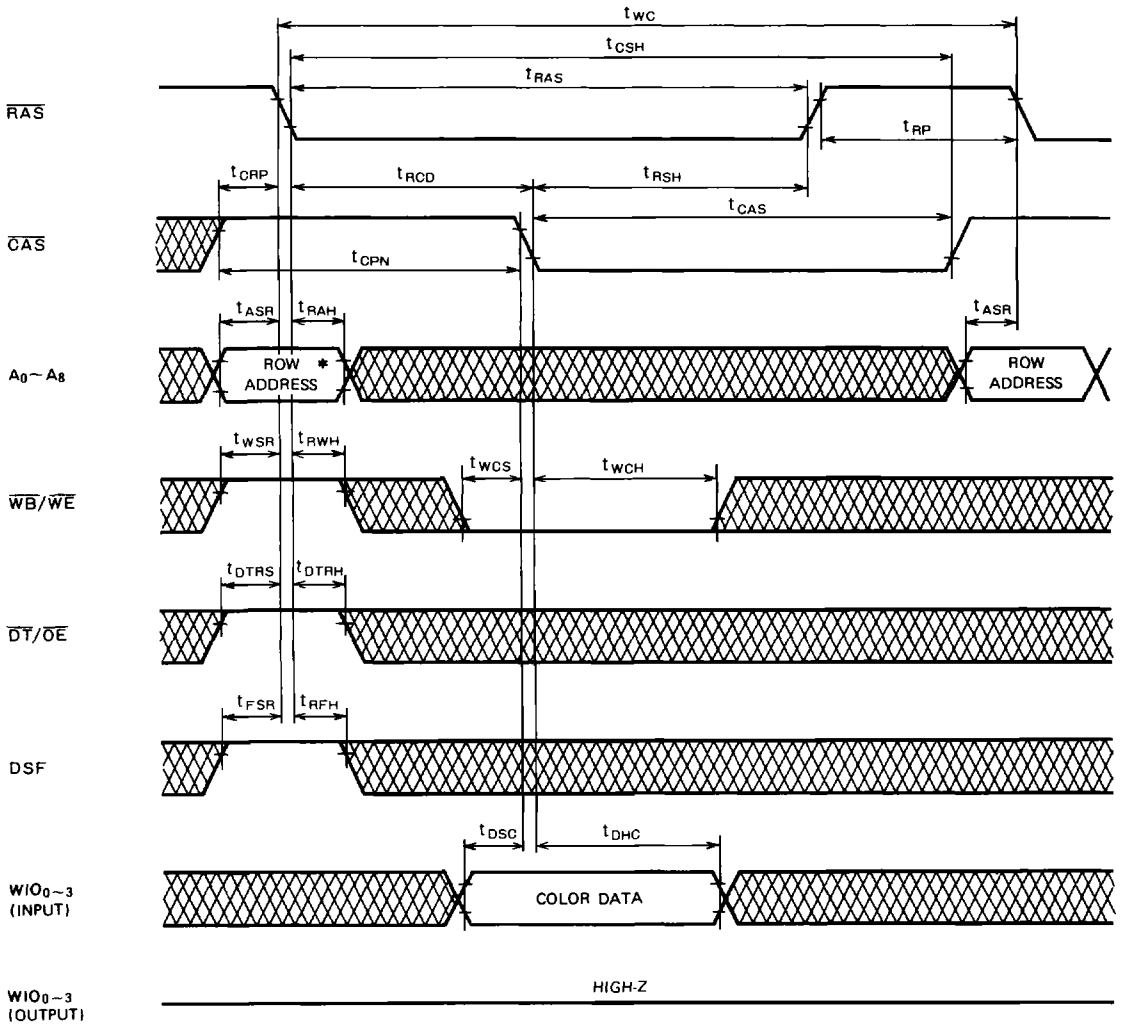
*L = Write per bit operation mask is effective during the continuous page mode cycle.

Flash Write with Mask



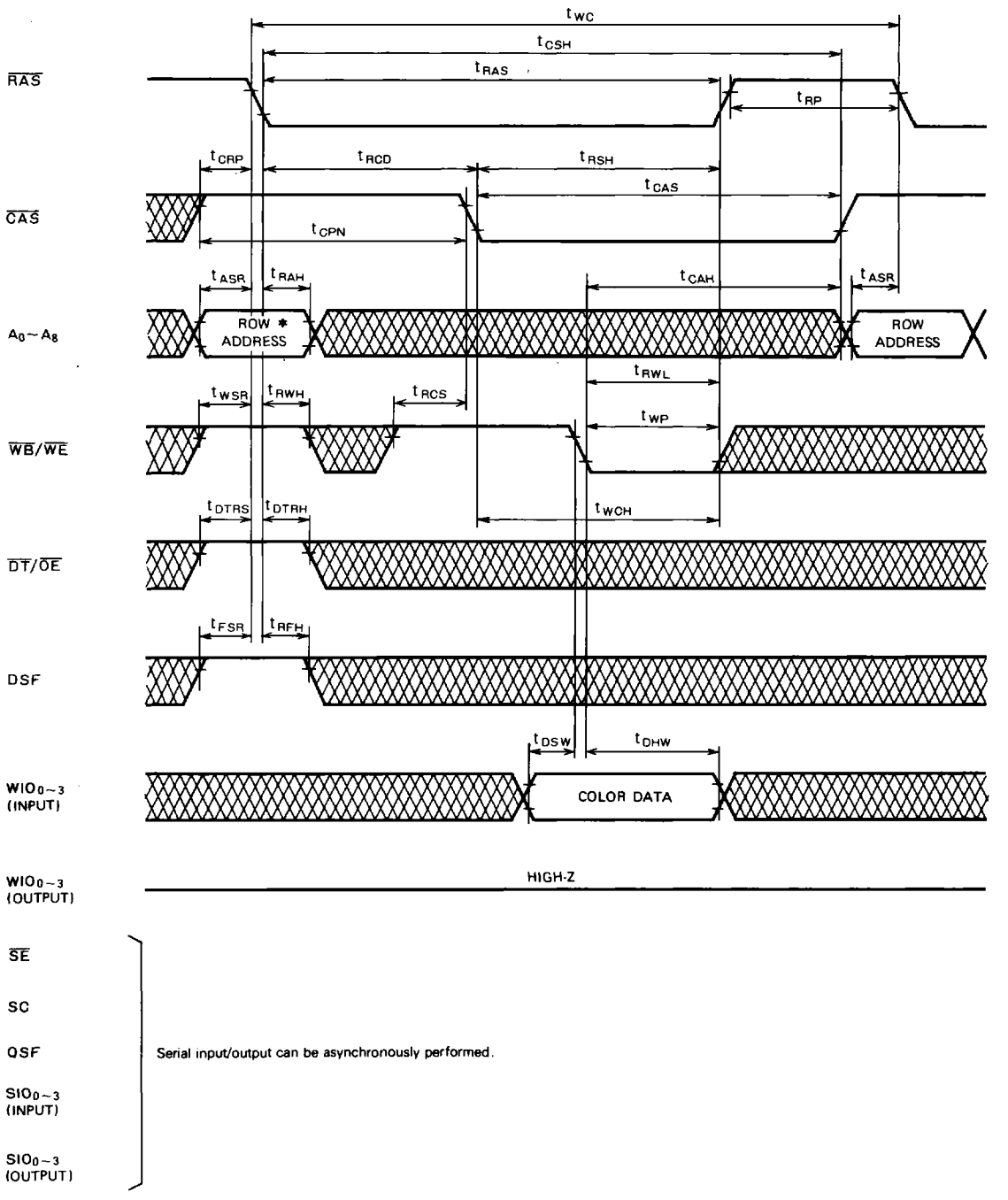
((Color Register data do not change during (after) flash white cycle))

Load Color Register Cycle (Early Write, $\overline{CAS}$ Latch Data)



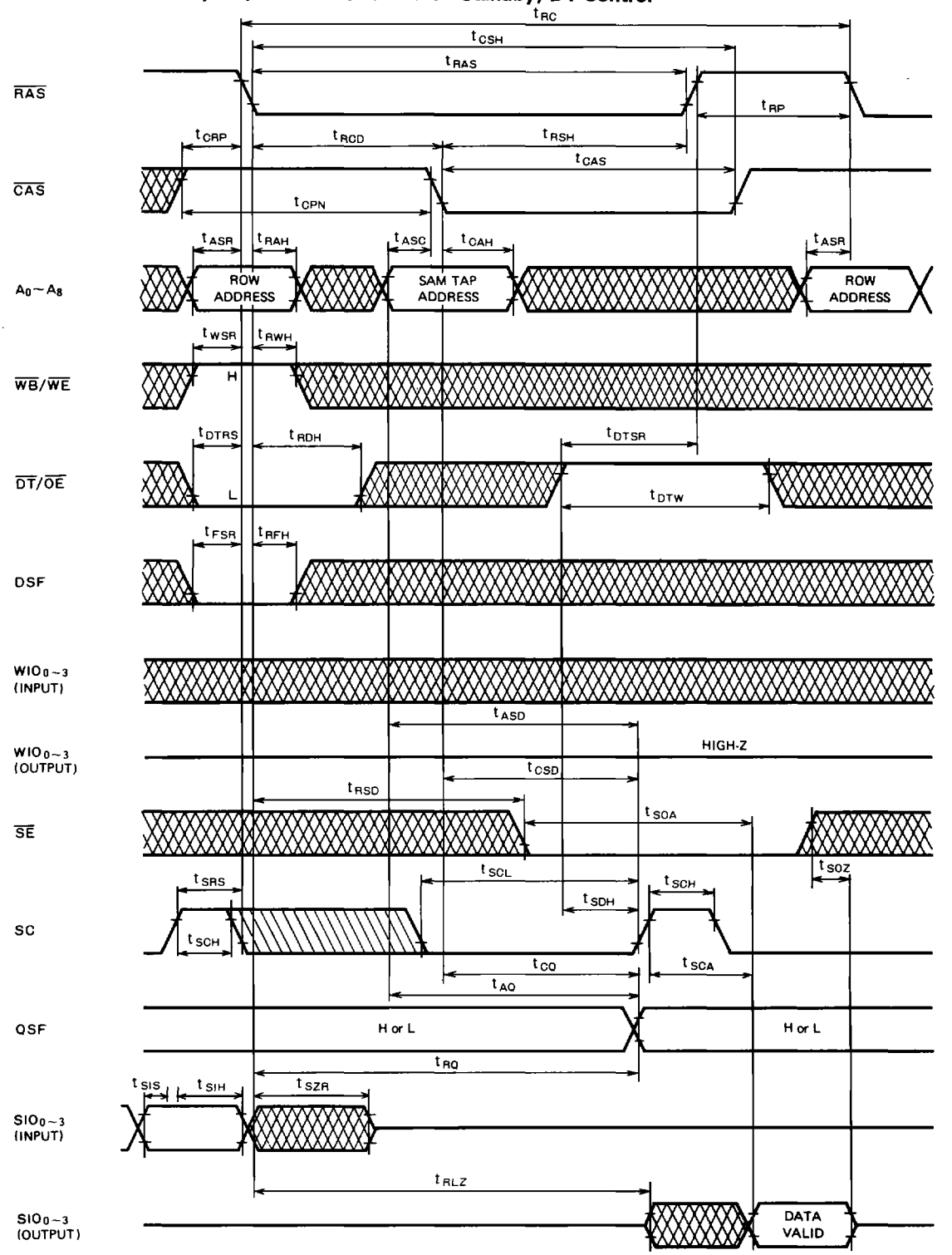
* For refresh address ($\overline{RAS}$ only)

Load Color Register Cycle (Late Write, Write Latch)

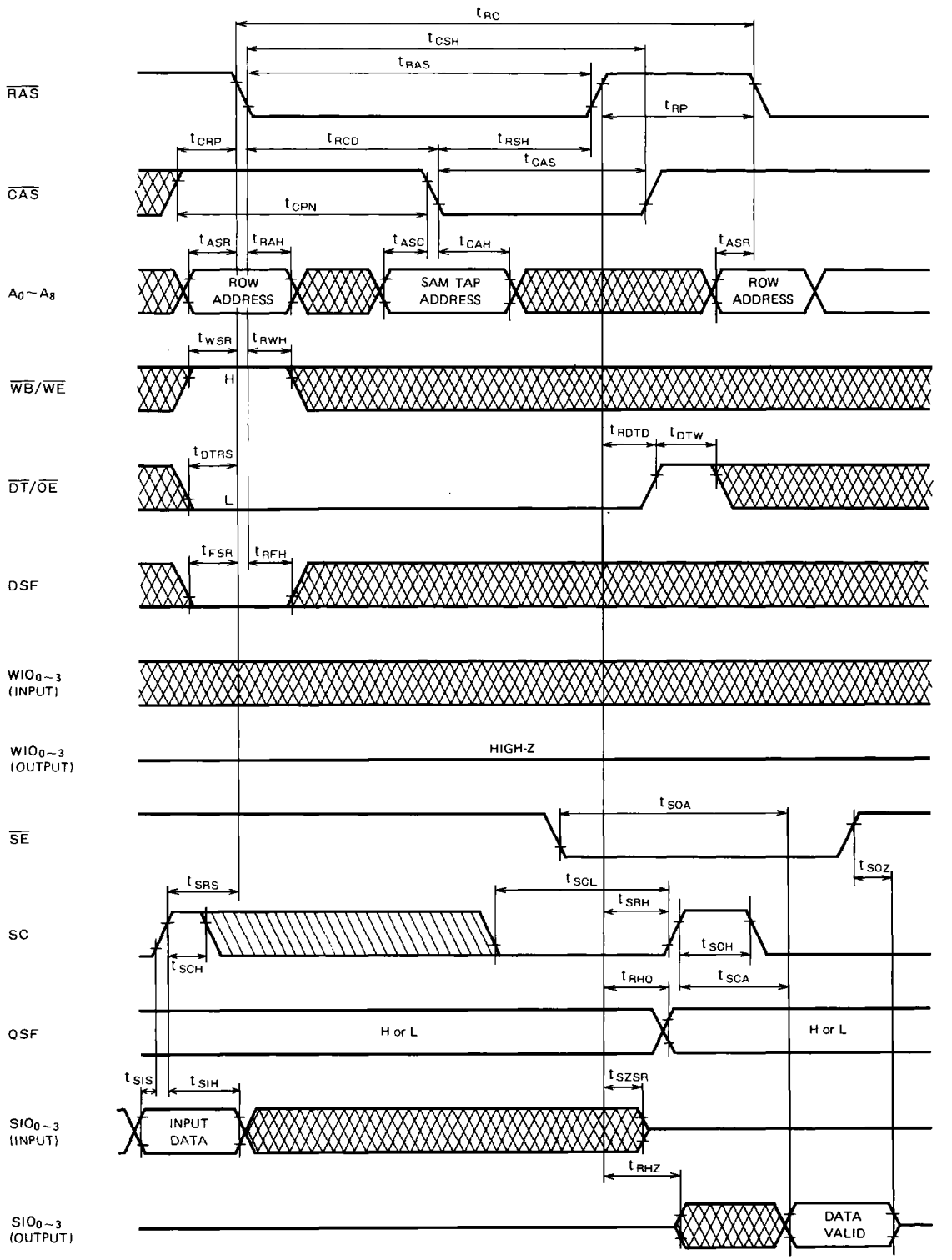


* For refresh address ($\overline{RAS}$ only)

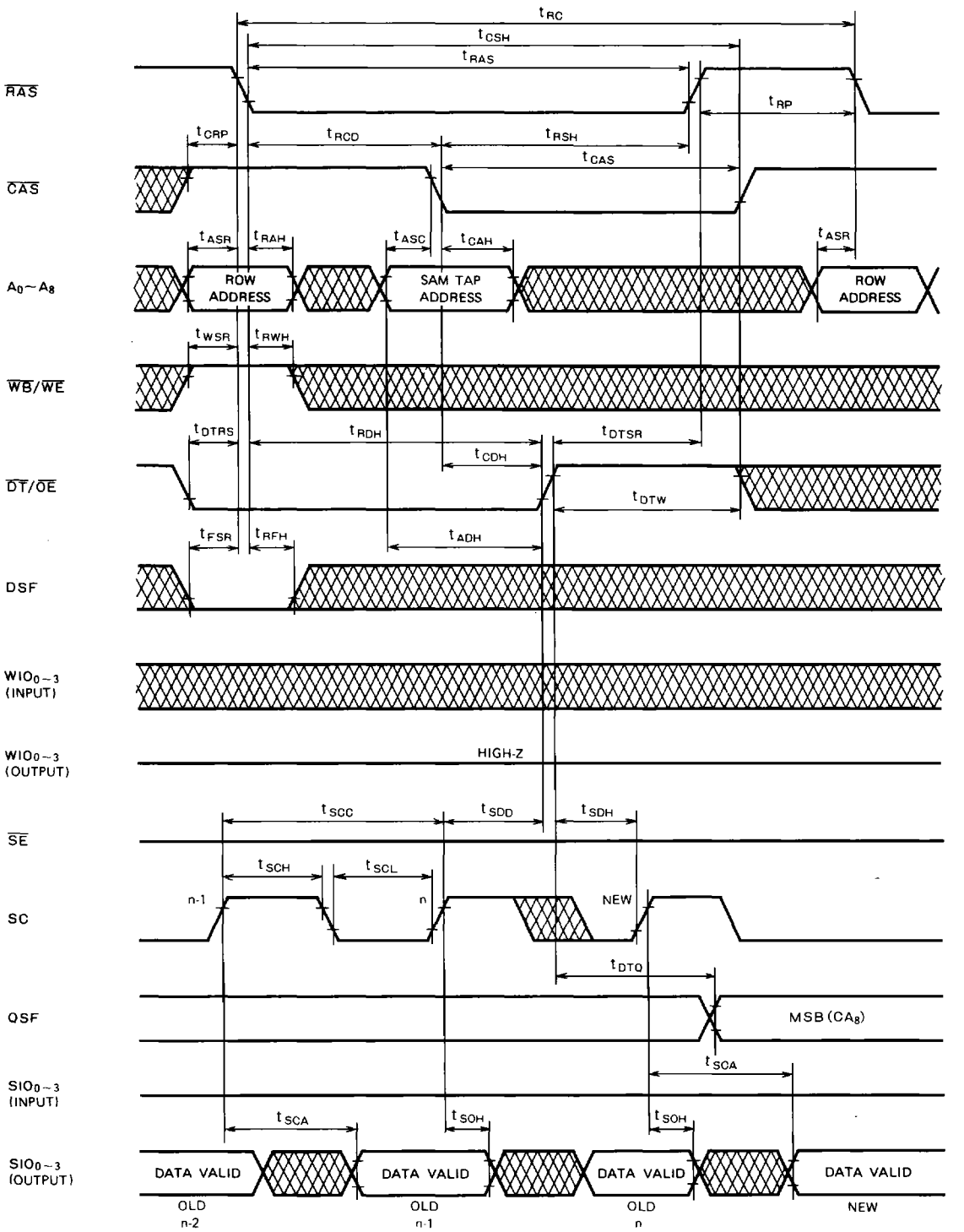
Normal Read Transfer Cycle (Pre-State: Serial Port = Standby) $\overline{DT}$ Control



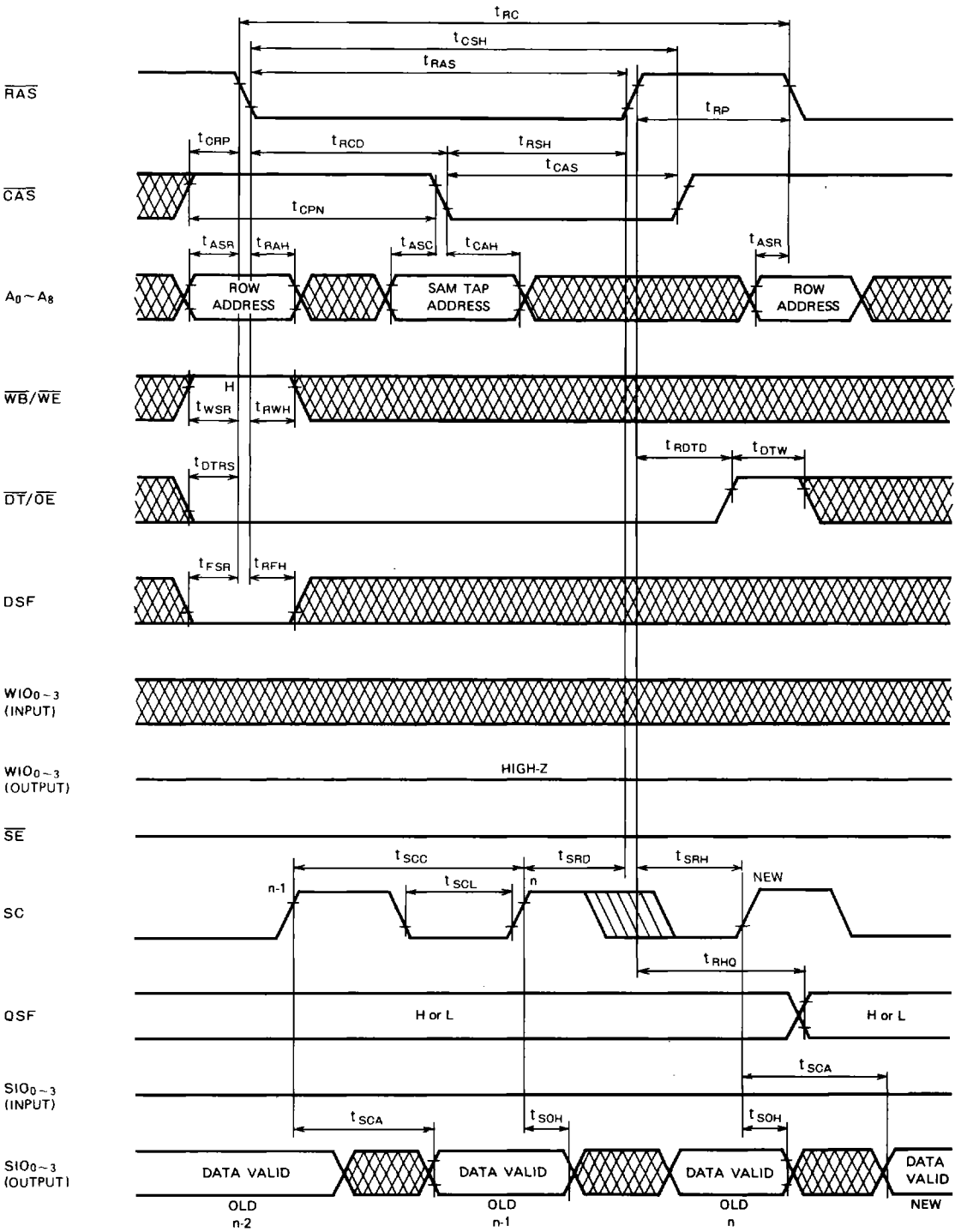
Normal Read Transfer Cycle (Pre-State: Serial Port = Standby) $\overline{RAS}$ Control



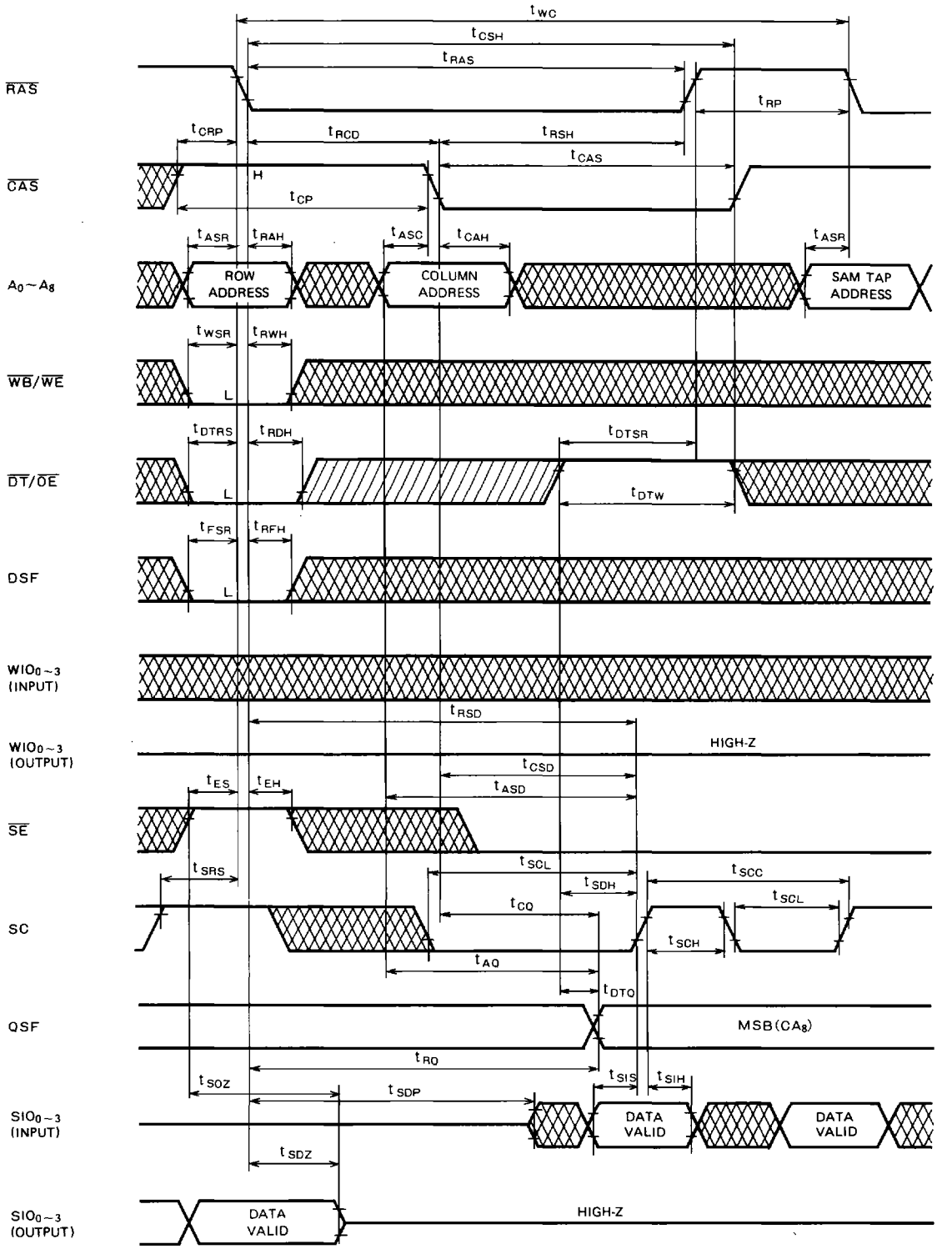
Real-Time Read Transfer Cycle (To Active Register; Serial Port Active) $\overline{DT}$ Control



Real-Time Read Transfer Cycle (To Active Register; Serial Port Active) $\overline{RAS}$ Control

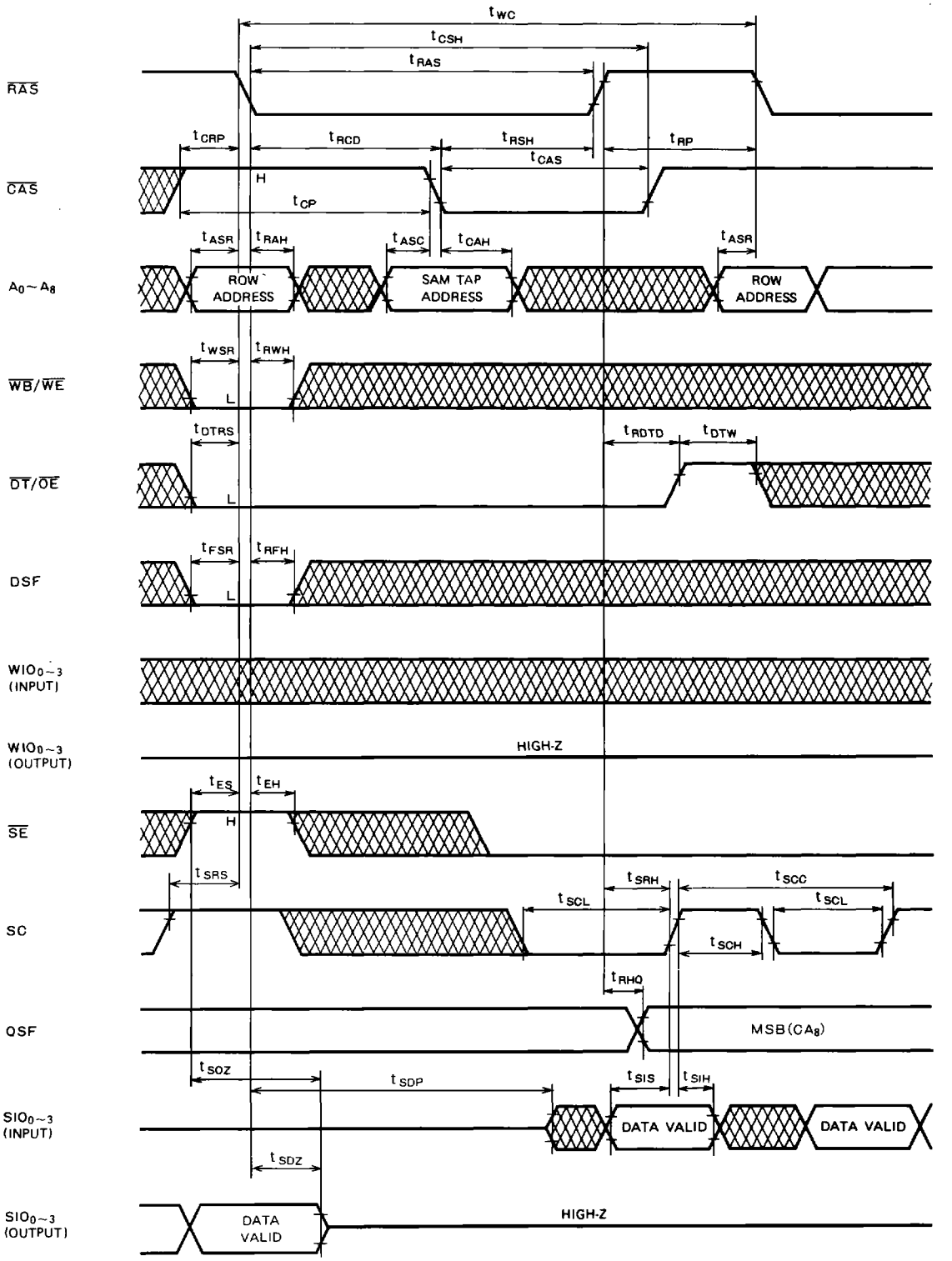


Pseudo Write Transfer Cycle (Serial Port Active) Serial Write Setup $\overline{DT}$ Control



Note When $\overline{SE}$ is "H" level, the serial input data are not written into the Data Register, but the serial data selector works.

Pseudo Write Transfer Cycle (Serial Port Active) Serial Write Setup $\overline{RAS}$ Control



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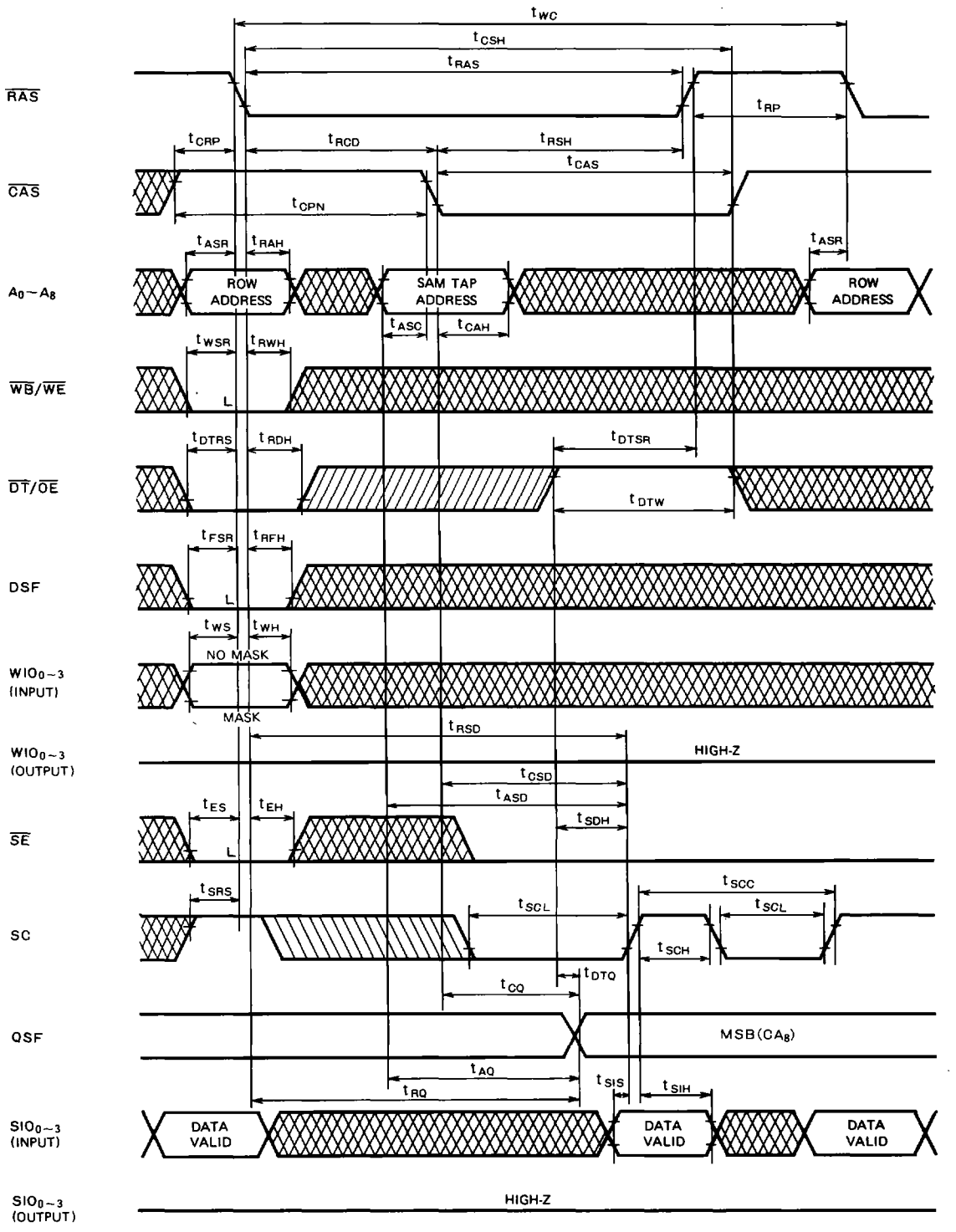
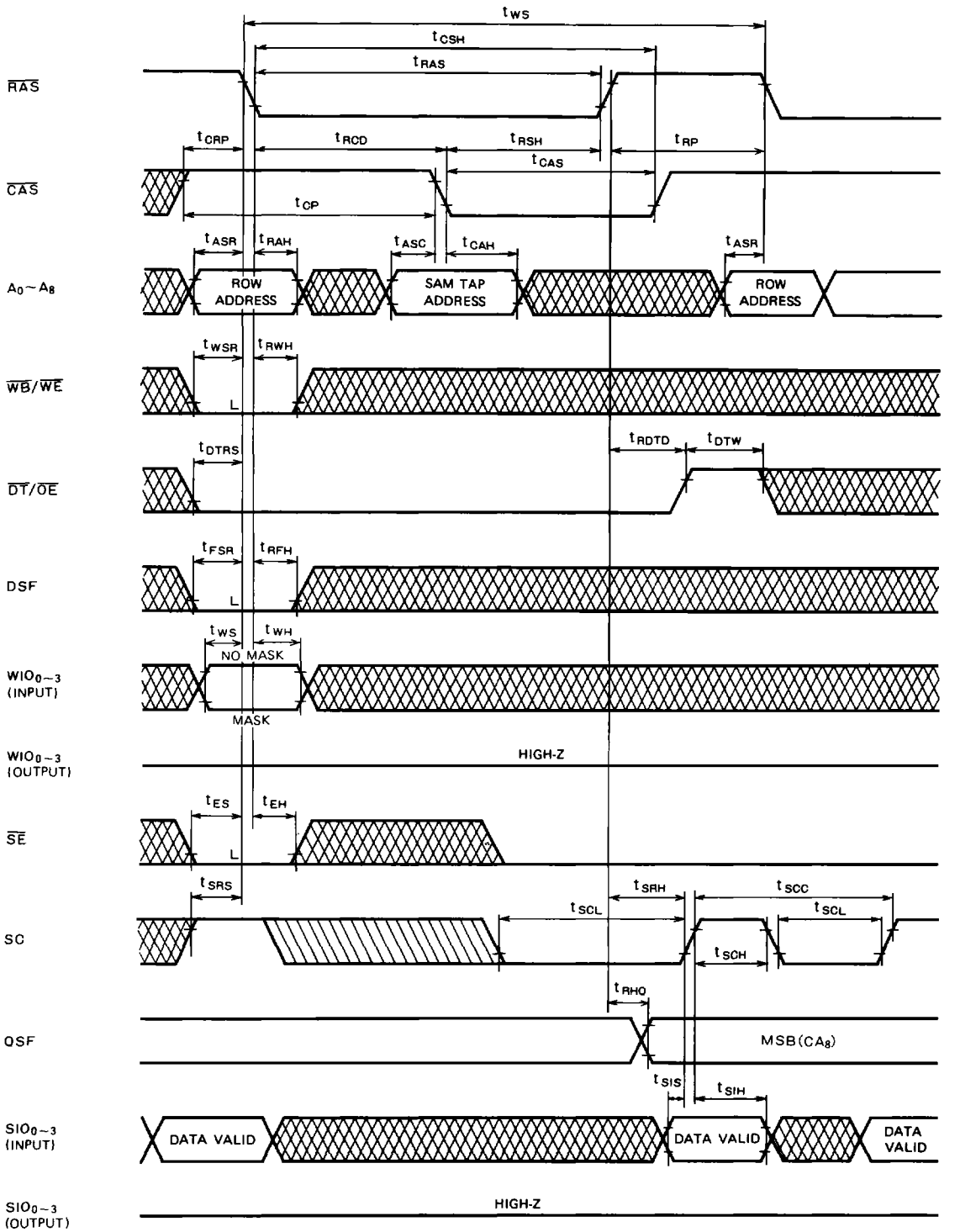
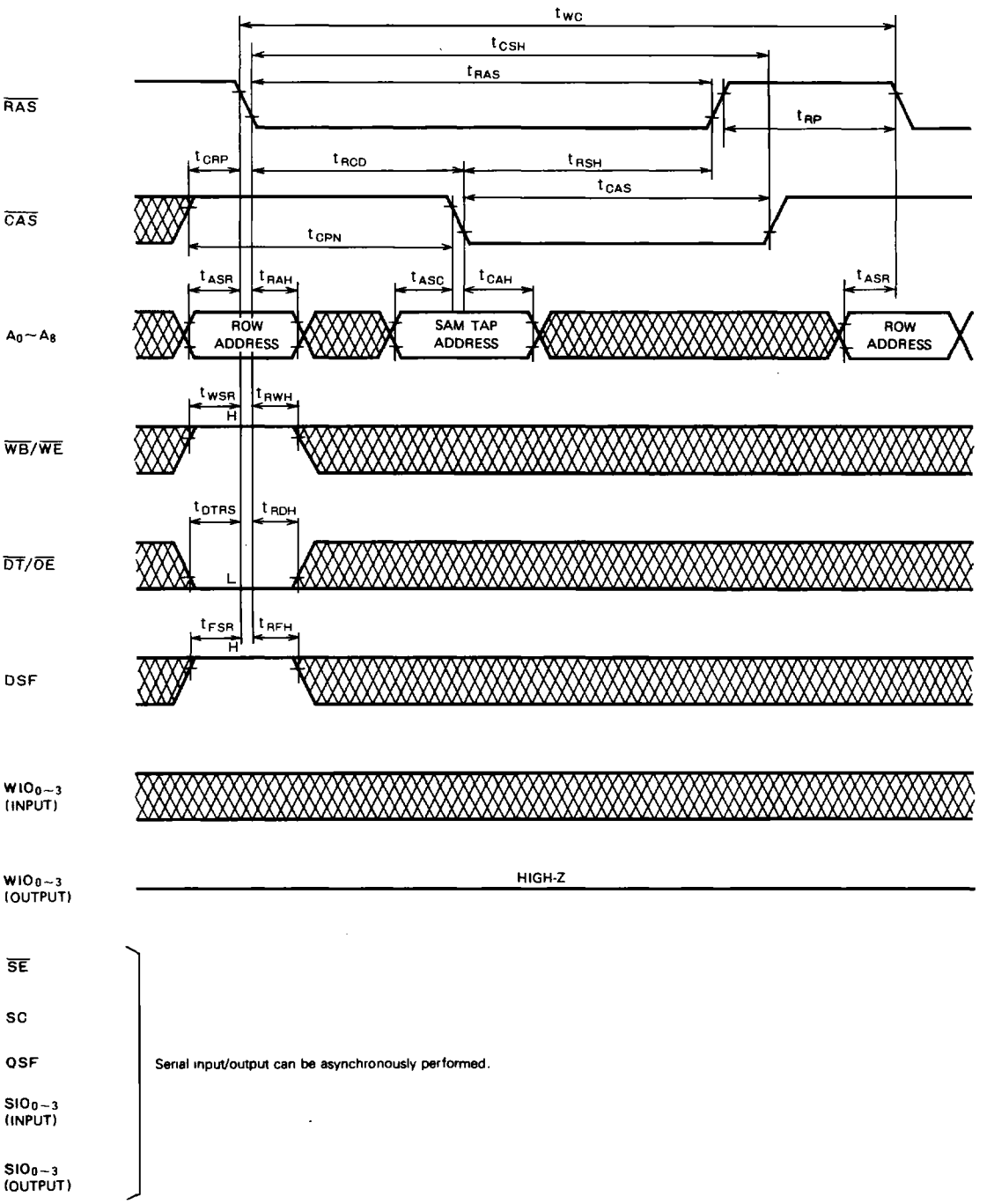
Write Transfer Cycle (Serial Port = Write Cycle) with New Mask $\overline{DT}$ Control



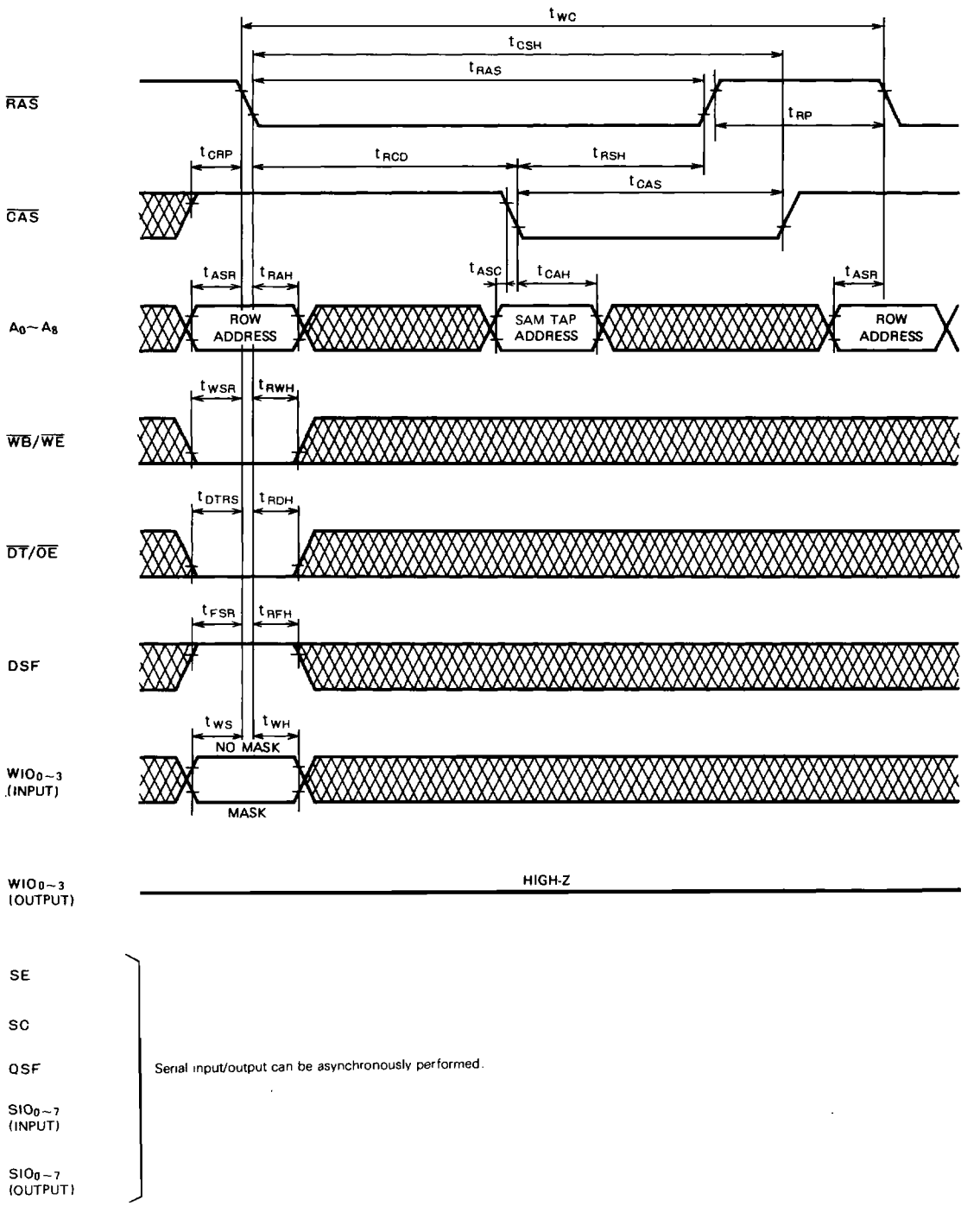
Write Transfer Cycle (Serial Port = Write Cycle) with New Mask $\overline{RAS}$ Control



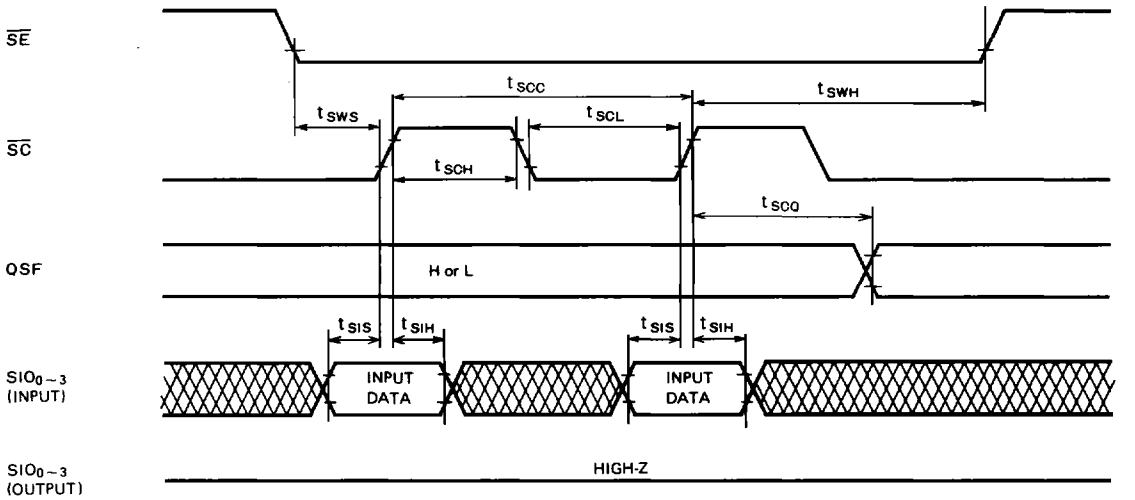
Split Read Transfer (to Inactive Register)



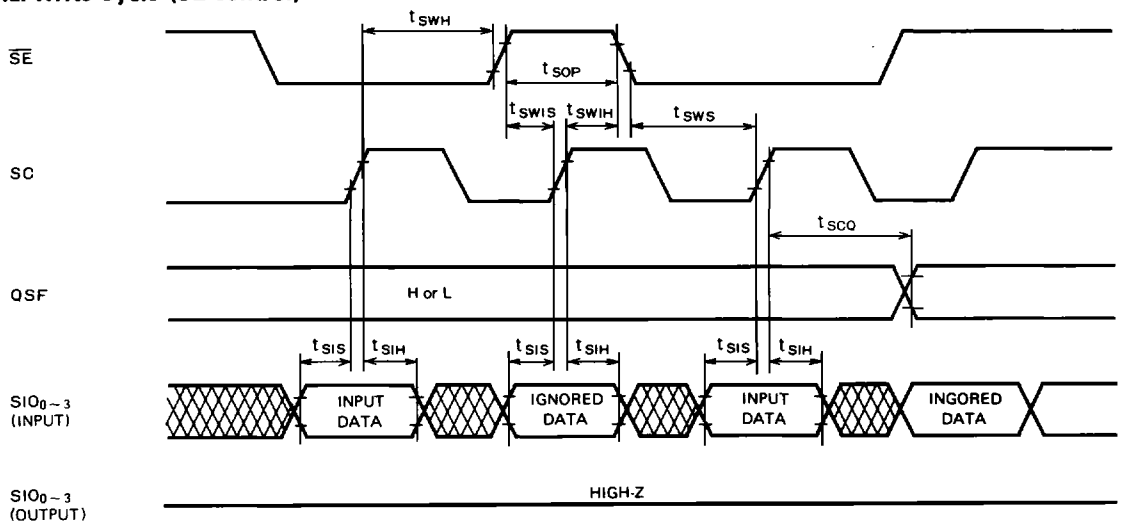
Split Write Transfer Cycle (to Inactive Register) with New Mask



Serial Write Cycle (SC Toggling, $\overline{SE}$ = L)



Serial Write Cycle ($\overline{SE}$ control)



Serial Read Cycle