- **Single-Chip ISO-MPEG (Layers 1 and 2) Audio Decoder**
- **Decodes Mono, Dual, Stereo, and Joint Stereo Modes**
- **Supports All MPEG Sampling and Data Rates, Including Free Format**
- **Complete With Stereo Level Control**
- **Input May Be MPEG Audio Frames or the Full-Multiplexed MPEG System Stream**
- **Accepts Compressed Audio at up to 15-Mbits/Second Burst Rate**
- **Bit-Serial or Byte-Parallel Compressed Data Input**
- **16- or 18-Bit Serial PCM Output Directly Interfaces to Most Serial D/A Converters**
- **8-Bit Microprocessor Control Interface**
- **Optional DRAM Interface for Audio Delay and More Robust Error Concealment**
- **Low-Power Submicron CMOS Technology, Fully TTL Compatible**
- **Small Footprint 120-Pin Plastic Quad Flat Package**
- **IEEE Standard 1149.1 (JTAG) Compatible**

description

The Texas Instruments TMS320AV110 MPEG audio decoder implements in a single chip, the International Standards Organization — Moving Picture Expert Group (ISO-MPEG) audio decompression algorithm. The ’AV110 accepts an MPEG-compliant compressed audio stream at any of the valid MPEG data and sampling rates and produces decompressed 2s complement audio output in either 16- or 18-bit serial pulse-code modulation (PCM) format. The PCM data stream is suitable for direct input to most commercially available digital-to-analog (D/A) converters.

Both MPEG layers one and two are implemented. The ’AV110 decodes a single monaural channel, two independent mono channels, stereo channels, and joint stereo channels. The compressed audio may be input either as MPEG audio frames or as the full-multiplexed system stream containing multiple audio and/or video packets. The input may be at the actual bit rate or it may be in bursts at up to 15 Mbits/s.

Compressed audio may be input in either bit-serial or byte-parallel formats. An eight-bit microprocessor interface is provided for control and status register access with maskable interrupts for the critical status and error flag registers.

While the ’AV110 can operate as a single, stand-alone decoder, provision is also made for using a 256K×4 DRAM device if buffering of the audio stream is required. With the external memory in place, audio may be buffered for synchronization purposes. The external memory also allows the employment of more robust error-concealment techniques if cyclic redundancy check (CRC) or synchronization errors are detected by the decoder.

The TMS320AV110 is implemented in the Texas Instruments EPIC™ CMOS submicron, triple-level-metal technology.